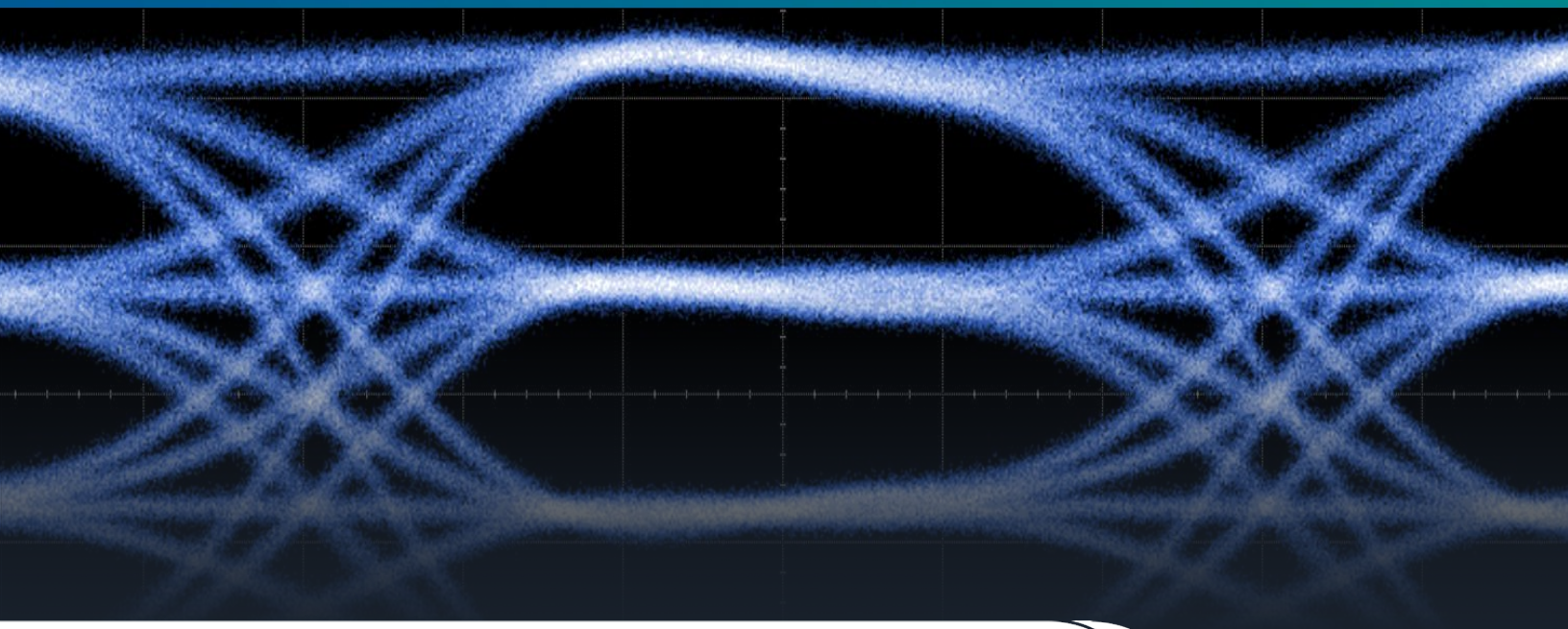

WHITE PAPER

What is a Bit Error Ratio Tester?

Fundamentals Series

A Bit Error Ratio Tester (BERT) is a piece of electronic test equipment used to measure BER in a data transmission system. A BERT includes a pattern generator and an error detector and is used to perform design verification, characterization, compliance, and manufacturing test of high-speed communication ports for ASICs, components, modules, and line-cards in the semiconductor, computer, storage, and communication industries.

Figure 1: Keysight's M8040A 64 GBaud High-performance BERT

Keysight's M8040A BERT is designed for R&D and test engineers who characterize chips, devices, transceiver modules, and sub-components/boards/ systems with serial I/O ports operating with symbol rates up to 32 and 64 GBaud.

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What Does a BERT Measure?

When you transmit data from one location to another, there are errors introduced due to a variety of factors including signal to noise, distortion, and jitter. Being able to measure these errors is critical to understanding the quality of your digital transmission system. One way to do this is to measure the bit error ratio, or BER.

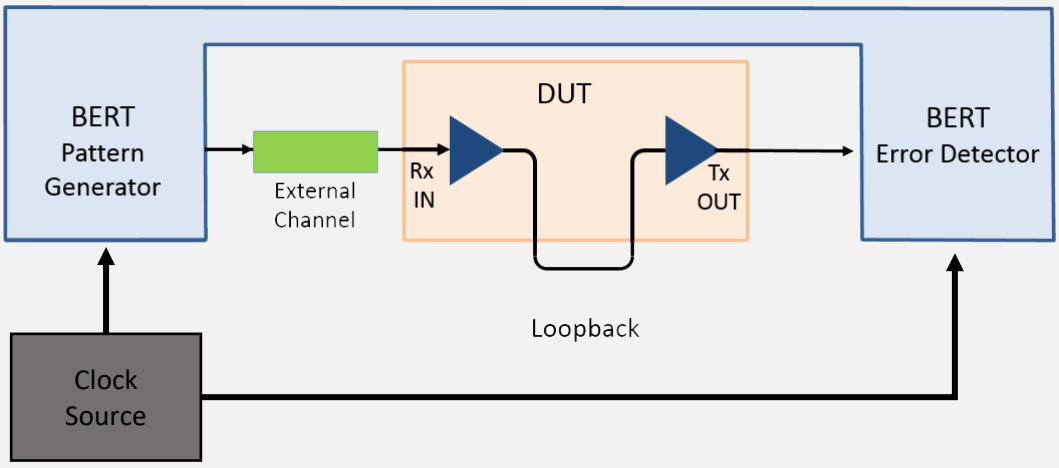
BER is calculated by comparing the transmitted sequence of bits to the received bits and then counting the number of errors. The ratio of how many bits received in error over the total number of bits received, is the BER.

$$BER = \frac{N\ Err}{Nbits}$$

BERTs are used to measure the bit error ratio of a digital transmission system. Historically, BERTs were used to characterize both transmit and receive physical layer performance. But this testing transitioned to focus more on testing the receive side with stressed signals provided from the BERT. The test results also provide a measure of things like total jitter, jitter tolerance, interference tolerance, and the sensitivity of your receiver.

How Does a BERT Measure the Bit Error Ratio?

To fully understand how a bit error ratio tester works, let's first walk through the diagram below. Both the pattern generator and error detector are driven from the same internal clock source. The pattern generator sends your selected pattern to the transmitter of the system under test. The receiver of the device under test (DUT) sends the data back to the BERT error detector. The BERT is then able to calculate the error rate relative to the bits transmitted and received (i.e. the bit error ratio).



Now that you understand how a BERT measures bit error ratios at a high level, let's dive deeper into each component.

Pattern Generator

The pattern generator transmits a defined test pattern to the system under test. Pattern generators can source signals at many data rates, from kilo-baud rates to Gigabit rates. The pattern can also be a packet of data that will be compared to what was received at the error detector. The pattern generator creates this test pattern together with a separate clock signal at the selected data rate and sends it to the DUT. Higher-end pattern generators (multi-gigabit) also provide the clock source, but de-emphasize capability and jitter injection.

Clock Source

The clock source is used to synchronize the pattern generator and the error detector. BERTs have very accurate time bases and timing circuits. These circuits are controlled by either an internal clock or an externally supplied clock. Often, a lower frequency reference clock can be applied to the BERT and then multiplied to the target data rate by using a multiplying phase lock loop within the BERT.

The pattern generator and the error detector operate at identical clock rates and the phase relationship between them must be stable. The best way to ensure this is to use the pattern generator's clock as the clock source for the error detector. This is easy enough when the two units are in close physical proximity – a direct electrical connection can be made between them. When the pattern generator and the error detector are on opposite ends of a transmission link, a direct connection may not be possible. In this case, the error detector's clock signal must be recovered directly from the data received by the error detector. However, if the system under test has re-timing circuitry, the pattern at the error detector's input is sampled with its internal clock. The position of the sampling point should be in the center of the eye, and the phase between the sampling clock and the data pattern should be aligned. This is a good rule of thumb in case jitter is present on the data pattern. In addition, the jitter phase of the data and the clock should be aligned to avoid errors caused by incorrect clocking.

Error Detector

The error detector uses its own generator that produces an exact replica of the pattern generator's transmitted test pattern. It then compares every received bit against this internally generated pattern. An error is detected each time the received bit differs from the known transmitted bit. However, the expected pattern into the error detector can also be defined independently from the pattern generator's output. This is an important BERT feature because popular interface technologies like USB, PCIe, and SATA remove filler symbols and insert their own filler symbols to compensate for the clock differences between the device and the host. Because of this, the error detector must be able to detect these inserted symbols and ignore the filler symbols during error counting.

Where Are BERTs Used?

BERTs are used for a wide range of applications:

- R&D and test engineers who characterize/verify compliance of chips, devices, boards, and systems with serial I/O ports use BERTs. They are used to test popular serial bus standards, such as: PCI Express, USB, MIPI M-PHY, SATA/SAS, DisplayPort, SD UHS-II, Fibre Channel, memory buses, backplanes, repeaters, active optical cables, Thunderbolt, 10 GbE, 100 GbE (optical and electrical), SFP+, CFP2/4 transceivers, CEI.
- Receiver (input) testing for many popular interconnect standards that use PAM-4 and NRZ data formats, such as: 400 GbE, 50/100/200 GbE, OIF CEI-56G, and CEI-112G, 64G/112G Fibre Channel, proprietary interfaces for chip-to-chip, chip-to-module, backplanes, repeaters, and active optical cables.
- Mobile and Digital Video: USB, SATA, MIPI, DP, HDMI, SD, TBT
- Computing/Server – Front side bus, Memory Bus PCI Express, Hyper Transport, QPI, SAS
- Data Center/Cloud – Networks: Ethernet, Fibre Channel, Ethernet 10G, OIF CEI
- Communications – Long haul, Access, Wireless backbone: Ethernet, PON, CPRI. Electrical, and optical.
- Aerospace Defense – Radar, Sat Comm

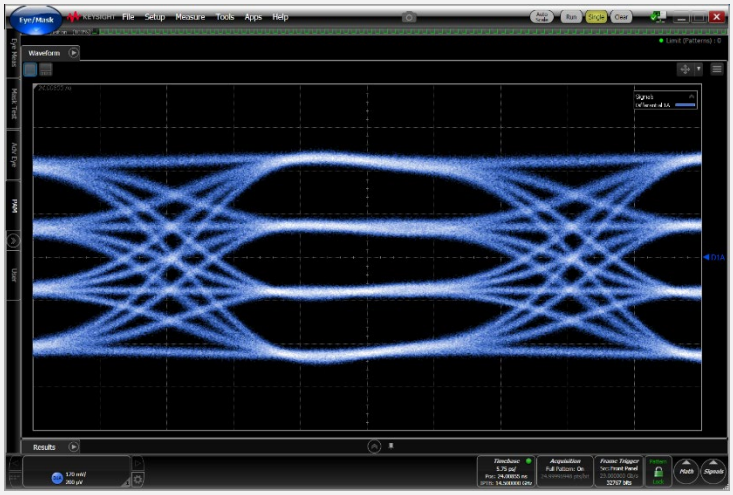


Figure 4: Keysight's M8040A, 64 GBaud BERT Pattern generator provides a clean 29 GBaud PAM-4 output signal

Conclusion

BERTs are an extremely valuable tool in measuring the quality of your digital transmission system. With built-in pattern generators, clock recovery systems, and error detectors, you can take your transmitter or receiver testing to the next level.

To learn more, read additional white papers in the *BERT Fundamentals Series* or visit the Keysight BERT website.

Learn more at: www.keysight.com

For more information on Keysight Technologies' products, applications or services, please contact your local Keysight office. The complete list is available at: www.keysight.com/find/contactus

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