

# Memory Analyzers

MA4100 Series Memory Analyzer Datasheet



# **New Features!**

- Supports JEDEC Engineering Procedures JEP175 DDR4 Protocol Checks published July 2017
- Updated real-time margin testing to the latest JEDEC specification JESD79-4B published June 2017
- Load-Reduced DIMM support (LRDIMM) enables up to 16 ranks per DIMM
- Second slot support enables monitoring of a dual channel with one instrument simultaneously
- More additions to the popular real-time performance measurements
- Create your own margin tests and find elusive problems

# **Key Performance Specifications**

- DDR4-3200
- Connects to any DDR4 target
- Continuous acquisition across clock stops and clock frequency changes
- 1G-sample acquisition depth

- Programmable probe termination
- 11ps x 10mV x 40-channel analog characterization (iCiS™)
- Real-time memory performance metrics
- Real-time memory compliance margins and validation
- Trigger in and trigger out

# **Key Features**

- Integrated Windows 7 Controller
- Application software ready for bench, remote-to-lab or offline operation
- Application includes advanced listing, waveform, tables and charting
- Turnkey setup, including automated MRS capture and analysis
- Analyze thousands of real-time memory parameters
- Full featured, industry standard trigger system
- Automated analysis runs for everything from detailed setup information, to quick summary runs, to in-depth extended data logging or margin testing runs
- Analog eye characterization on 40channels simultaneously at 11ps x 10mV
- Correlate with an oscilloscope for memory DQ data capture
- Patented interposer/probe designs
- Support for DIMM, SODIMM, miniDIMM, and/or x4/x8/x16 component interposers

## Applications

- DDR4 and/or DDR3
  - Memory validation and debug
  - Monitoring bus traffic
  - o Bus traffic measurement
  - Optimization of memory performance
  - Analog insight
- DDR4 rates to DDR4-3200
- DDR3 rates to DDR3-2667 (1.6GHz state clock capable)

## **Results Overview**

#### Real-time Continuous Analysis

Real-time analysis provides data results during and after analysis runs which may be extremely long (days) or very short (nanoseconds). During the run, analysis is continuous and in real-time. Any event that occurs during the run is captured and analyzed.

#### Performance

Memory performance metrics include realtime margin metrics and margin violations. For each margin test, results indicate test coverage, observed margin values, as well as flags indicating margin violations. All data is continuously acquired in real-time with results updates continuously while the analyzer is still running.

2		Prohing Setup	Memory Setup	Aca, Contro	I 🖏 Sectio	n Control 🚳	Performance & L	ogic Centure(t)
	names for	Logic Capture(s) (The Li	iting 🔽 Wavefu	erro 🥅 Rew D	ata 🚍 Vic	lations 🐻 Corr	plance Nevigator	Rev Statistics of Charls Resorts
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el	below i	nformation is for 1	Timing Set:					
t.	Index	Name	Status	Min.	Max.	Margin	Spec. Value	Description
	21	SOPR	08 28 00	NA	NA	NA	522 ok	Exit reset to a valid command.
	22	1003		760 ck	NA	40%	522 ck	Exit self-refresh to commands not requiring a locked DLL.
	22	DDS_fest		155 ek	NA	-38%	2.52 ck	Enit Self Refresh to ZQCL, ZQCS and MRS.
	22	SCHOLL		760 ck	NA	-196	760 ck	Ent Self Refrech to commands requiring a locked DLL.
	23	60P		6 ck	NA	0%	6 ck	Ent power down to valid command
	24	TCKESR		33 ck	NA	43795	6 ok	Minimum clock enable during self-refresh or minimum self-refresh time.
	25	SCIER		5 ek	NA	0%	5 ck	Clock enable minimum pulse width.
	27	(PDmar	81.80	NA	NA	NA	70,200 ck	Mazimun power down time.
	28	SACTPDEN		82 ck	NA	8,100%	1 ck	Activate to powee-down entry time.
	29	(PSPDEN		1 ck	NA	0%	1 ck	Precharge single or all banks to power-down entry time.
	30	<b>IRDPDEN</b>		70 ck	NA	84%	38 ck	Read with or without auto-precharge to power-down entry time.
	31	SWRPDEN		79 ck	NA	52%	52 ck	Write with a burst length of 3 to power-down entry time.
	32	IWRAPDEN		19,249 ck	NA	37,643%	51 ck	Write with auto-precharge and a burst length of S to power-down entry time.
	33	SWRPDC4DEN		79 ck	NA	38%	50 ck	White with a burst length of 4 to powes down entry time.
	34	tWRAPEC4DEN	00 31 90	NA	NA	NA	49 ck	Write with suto-precharge and a burst length of 4 to power-down entry time.
	35	TREFPDEN		147 ck	NA	14,600%	1 ck	Reflesh to power-down entry time.
	36	MESPDEN		9,027 ek	NA	37,513%	24 ck	MES to power-down entry time.
	37	tRA3nin	31.90	NA	NA	NA	30 ck	Minimum row active time or activate to precharge command period.
	38	(RASpar	00 00 R5 R0	NA	NA	NA	70,200 ck	Maximum row artirre time or activate to prechange command period.
	39	sRC		44 ck	NA	2%	43 ck	Row cycle time of activate to activate/refresh command period.
	40	19CD	31 50	NA	NA	0	0 ek	Activate to read or write time.

Memory performance metrics also include continuous real-time charting of bus performance characteristics such as throughput, utilization, power management, and more.



## Simultaneous State Capture

State capture results include continuous traffic around one or more events of interest. The traffic - consisting of time, bus commands, bus addressing, margin violations, and trigger events - is presented in listing or waveform displays. State capture depths from one hundred samples to one billion samples is available. Advanced acquisition controls monitor and respond to the continuous traffic in real-time to best utilize the state capture memory. Advanced post-capture search and filter can quickly parse the acquisition store.

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	918	4,055.24	2.25	0x2E8	0.0	1.2	RD8	0			ьос
	924	4,059.73	4.49	0x2E0	0.0	0.2	RD8	0			р00
	930	4,064.22	4.49	0x2E8	0.0	0.2	RD8	0			ь00
	936	4,068.71	4.49	0x2D8	0.0	1.2	RDS	0			ь00
	942	4,073.20	4.49	0x2D0	0.0	0.2	RDS	0			ь00
	948	4,077.69	4.49	0x2E0	0.0	1.2	RDS	0			ь00
	954	4,082.19	4.49	0x2D8	0.0	0.2	RDS	0			ь00
	960	4,086.68	4.49	0x2C8	0.0	0.2	RD8	0			b00
	966	4,091.17	4.49	0x2D0	0.0	1.2	RD8	0			ьо
	979	4,100.90	9.73	0x2F8	0.0	0.3	WR8	0			ь00
	983	4,103.90	2.99	0x2E0	0.0	3.1	WRS	0			ьо
	987	4,106.89	3.00	0x2F0	0.0	0.3	WRS	0			ь00
	991	4,109.89	2.99	0x2F0	0.0	1.3	WR8	0			b00
	995	4,112.88	3.00	0x2E8	0.0	3.1	WR8	0			ь00
	999	4,115.87	2.99	0x2E8	0.0	1.3	WRS	0			ь00
	1,003	4,118.87	3.00	0x2D0	0.0	2.0	WRS	0			ьо
	1,006	4,121.11	2.25	-	0.0	0.2	PRE	-			ьо
	1,008	4,122.61	1.50	0x2F8	0.0	1.3	WR8	0			b00
	1,012	4,125.61	2.99	0x2D8	0.0	2.0	WRS	0			b00
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## **Reliable Connection**

Over twenty compatible interposers/probes are available for DDR4 and DDR3 designed to preserve analog signal characteristics and maintain compatibility with Tektronix equipment for DQ data bus analysis.



Interposers/probes available for DDR4 and DDR3 DIMMs, SODIMMs, miniDIMMs and components (x4, x8, or x16).



## **Automated Analysis**

Analysis is automated and continuous from the time the user clicks the Start button until the analysis session completes. While running, the session updates the application with real-time results. In the following image you can see real-time margins for all compliance parameters as well as a chart of read/write bus throughput. In this example, the analyzer is configured to continuously monitor acquire data until the first occurrence of a compliance violation occurs. That's three simultaneous measurements, each collecting/monitoring real-time data!



Quickly find, analyze and share intermittent problems.



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## **Turnkey Setup**

From first starting the software there are five easy steps to start gathering data. First click the *New* icon (1) and select the system file for the interposer/probe you are using. Next reset your target to ensure MRS data is sent. The analyzer will automatically acquire this information! Now click the *Memory* Setup button (2) to display the setup window. Then select the correct speed bin, rank count, and density (3). Last, click the *Update Memory Configuration* button (4) to apply the MRS data to the analyzer's setup. That's it. You are ready to start analyzing data!



Higher speed operation (clock rates above 1GHz) may require additional per channel

tuning using iCiS<sup>™</sup>. For all speeds iCiS<sup>™</sup> can also analyze whether bit errors can be expected over a configurable amount of time (from milliseconds to hours). iCiS<sup>™</sup> is an extra step that is not always required but provides detailed and invaluable insight of signal quality and expected performance for data acquisition you can trust.



# **Check Online for More Information**

Check online at www.nexustechnology.com for more information including video tutorials and whitepapers. Topics include:

- Oscilloscope Correlation
- TLA/Scope Correlation
- JEDEC Protocol Compliance Analysis
- Dual Instrument Architecture
- Detailed Interposer/Probe Information
- iCiS
- Triggering and State
- Violations and Margins
- And more

# **Available Configurations**

## **DDR4** Configurations

## NEX-MA4150-DDR4

Memory analyzer with DDR4 performance, margins and capture up to DDR4-3200 (1.6GHz) with 1G-Sample acquisition depth. Additional support for DDR3 available as an option.

#### NEX-MA4120-DDR4

Logic analyzer capture only up to DDR4-3200 (1.6GHz) with 512M-Sample acquisition depth. Options available for 1G-Sample, performance, and margins. Options also available to add DDR3 support.

#### NEX-MA4100-DDR4

Entry level memory analyzer with DDR4 performance, margins and capture up to DDR4-2667 (1.34GHz) with 512M-Sample acquisition depth. Options include 1G-Sample, and DDR4-3200 (1.6GHz) support. Options also available to add DDR3 support.

#### **DDR3** Configurations

#### NEX-MA4100-DDR3

Memory analyzer with DDR3 performance,

margins and capture up to DDR3-2133 (1.34GHz capable) with 512M-Sample acquisition depth. Option for 1G-Sample. Options also available for 1.6GHz state speed. Options also available to add DDR4 support at DDR4-2667 or DDR4-3200.

## **Contact Information**

For more information, please contact us by telephone, email or mail as listed below. Normal business hours are 9:00 - 5:00 EDT/EST.

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