# Keysight Technologies

## M8040A High-Performance BERT 64 Gbaud

## Data Sheet

Version 1.7

**NEW**

- Equalizer
- Analyzer up to 64 Gbaud NRZ
- Clock recovery
- RI/SI injection

Master your 400G design

KEYSIGHT TECHNOLOGIES

# Table of Contents

# Introduction

The Keysight Technologies Inc. M8040A is a highly integrated BERT for physical layer characterization and compliance testing.

With support for pulse amplitude modulation 4-level (PAM-4) and non-return-to-zero (NRZ) signals, and symbol rates up to 64 Gbaud (corresponds to 128 Gbit/s) it covers all flavors of the emerging 400/200 GbE and CEI-56G standards.

The M8040A BERT´s true error analysis provides repeatable and accurate results, optimizing the performance margins of your devices.

## Key features

- Data rates from 2 to 32 and 64 Gbaud
- PAM-4 and NRZ selectable from user interface
- Built-in 4 tap de-emphasis to compensate loss
- Integrated and calibrated jitter injection: RJ, PJ1, PJ2, SJ, BUJ, and clk/2 jitter
- Two pattern generator channels per module to emulate aggressor lane
- Linearity tests with adjustable PAM-4 levels
- Short connections to the DUT with remote heads for the pattern generator
- True PAM-4 error detection in real-time for low BER levels
- Built-in and adjustable equalization to re-open closed eyes
- Clock recovery with N1076A and N1077A
- RI and SI level interference injection via M8195A/96A AWG
- Graphical user interface and remote control via M8000 system software
- Scalable and upgradeable with options and modules

## Applications

The M8040A is designed for R&D and test engineers who characterize chips, devices, transceiver modules and sub-components, boards and systems with serial I/O ports operating with symbol rates up to 32 Gbaud and 64 Gbaud in the data center and communications industries.

The M8040A can be used for receiver (input) testing for many emerging interconnect standards, such as:

- IEEE 802.3bs 400 and 200 Gigabit Ethernet (200GAUI, 200GBASE, 400GAUI, 400GBASE)
- IEEE 802.3bj 100 Gigabit Ethernet
- IEEE 802.3cd 50, 100 and 200 Gigabit Ethernet
- OIF CEI - 56G (NRZ and PAM-4 versions)
- 64G/112G Fibre Channel
- Infiniband-HDR
- Proprietary interfaces for chip-to-chip, chip-to-module, backplanes, repeaters, and active optical cables, operating up to 64 Gbaud.

## M8000 Series of BER Test Solutions

### Simplified time-efficient testing is essential when you are developing next-generation computer, consumer, or communication devices

The Keysight M8000 Series is a highly integrated BER test solution for physical layer characterization, validation, and compliance testing.

With support for a wide range of data rates and standards, the M8000 Series provides accurate, reliable results that accelerate your insight into the performance margins of high-speed digital devices.

New: PAM-4 BERT
up to 64 Gbaud

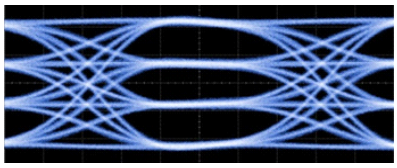


Figure 1. The M8000 Series BER test solution is highly integrated and scalable to address the test challenges of the next generation of high-speed digital receiver test.

The M8040A high-performance BERT 64 Gbaud extends the M8000 Series for 400G data center interconnect testing

# M8040A High-performance BERT 64 Gbaud

## Simplifies accurate receiver characterization of devices operating up to 32 and 64 Gbaud with NRZ and PAM-4 signals

## Highest level of integration streamlines receiver test setups

With the M8040A, all critical test capabilities for input/receiver (RX) characterization are built-in. The pattern generator module provides calibrated and integrated jitter sources and de-emphasis to emulate the transmitter (TX) and to compensate for channel loss in the test setup. In addition, the M8040A provides an internal clock synthesizer and a second pattern generator output channel to emulate an aggressor lane.

The analyzer provides true PAM-4 and NRZ error analysis in real time and full sampling to measure down to very low BER and SER.

This high level of integration with the M8040A makes the receiver test set-up connections easier and more robust. Set up and debug time is shortened, calibration is simpler and the frequency of re-adjustments is reduced, resulting in a more efficient use of overall test time.

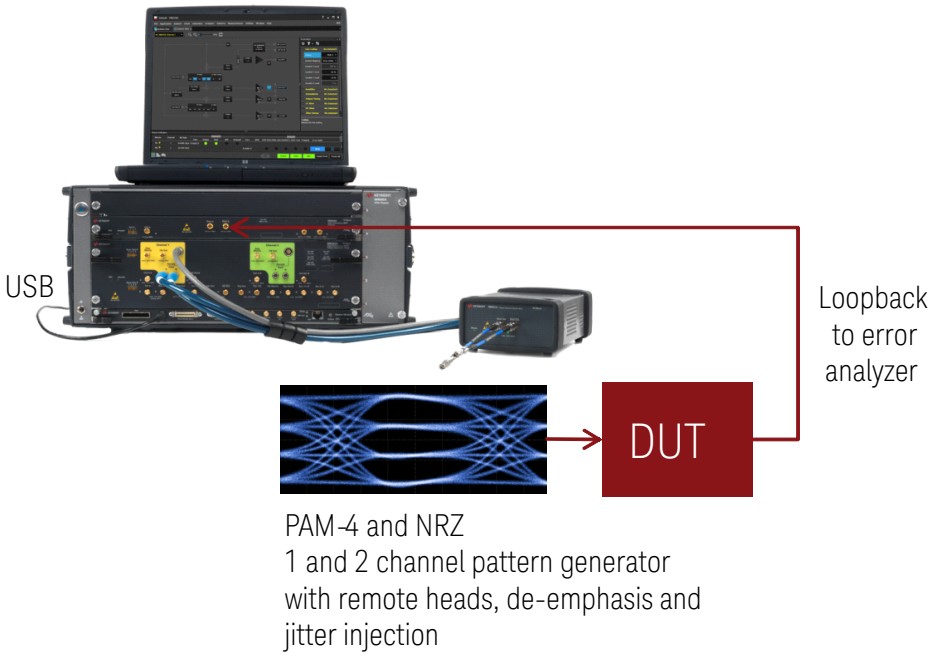



Figure 2. The M8040A streamlines complex receiver test setups. Each of the 1 or 2 pattern generator channels provides built-in de-emphasis, jitter sources, and a remote head to reduce the distance between the generator output and the DUT test board. The full sampling error analyzer can detect errors in real-time for NRZ and PAM-4 signals without the need to split up the PAM-4 signal for multiple error detector channels.

# Repeatable and accurate results with M8040A

The M8040A high-performance BERT provides clean NRZ and PAM-4 signals up to 64 Gbaud with fast transitions and low intrinsic jitter. The remote head concept of M8040A with the short 1.85 mm cables brings the performance close to the device under test, minimizing signal degradations caused by lossy channels.

Figure 3. The remote head M8057A is required for each channel and is required for NRZ and PAM-4 signals. It contains an adjustable gain amplifier without re-timer. Users can select NRZ or PAM-4 coding and de-emphasis taps settings from the user interface with no need to reconnect cables. The cable between the remote head and the module is 0.85 m long. This allows positioning the remote head closely to the test board for the device under test.

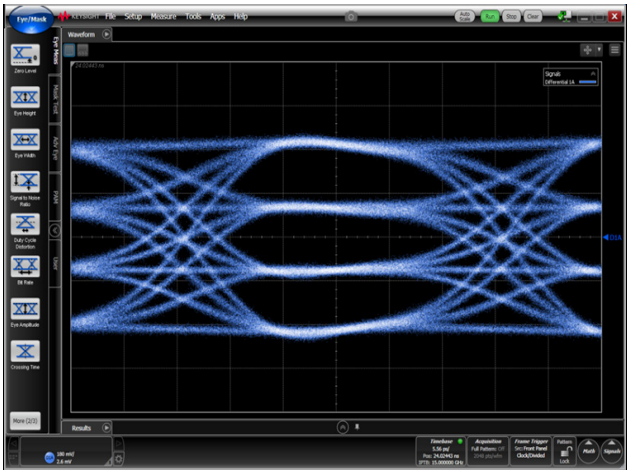


Figure 4. Clean 30 Gbaud PAM-4 output signal of pattern generator module M8045A with remote head M8057A using the internal clock source with 600 mV output amplitude and PRBS$2^{15}$-1. Measured with Infiniium DCA-X 86100D.

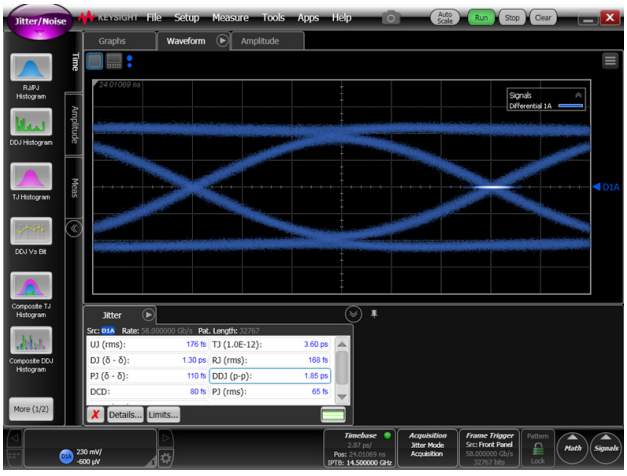


Figure 5. Clean 58 Gbaud NRZ output signal of pattern generator module M8045A with remote head M8057A using the internal clock source with 600 mV output amplitude and PRBS$2^{15}$-1. Measured with Infiniium DCA-X 86100D.

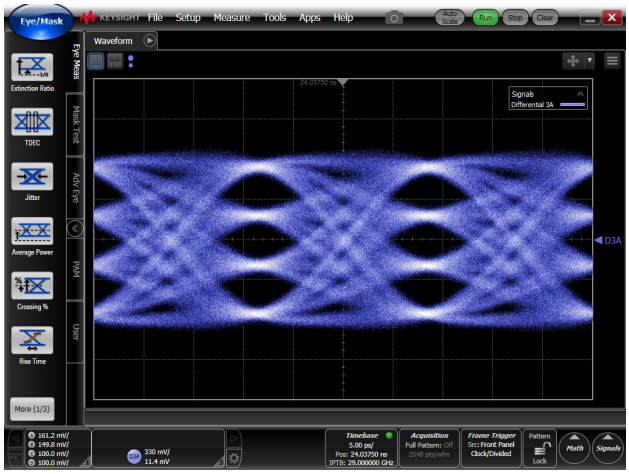
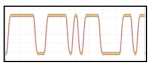
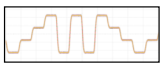


Figure 6. Clean 58 Gbaud PAM-4 output signal of pattern generator module M8045A with remote head M8057A using the internal clock source with 600 mV output amplitude and PRBS$2^{15}$-1.

# Emulate stress conditions for NRZ and PAM-4 input tolerance testing with M8040A

M8040A provides all capabilities required for input tolerance test:

- 1 or 2 channels. Second channel can be used as aggressor lane to emulate crosstalk effects
- Data rates are adjustable from 2 Gb/s NRZ up to 64 Gbaud PAM-4, selectable NRZ or PAM-4
- Algorithmic PRBS, QPRBS and memory-based patterns, pattern sequencer with loops, error injection
- Built-in and calibrated jitter sources that can be used simultaneously: RJ, multi-UI low-frequency jitter, multi-tone high-frequency jitter, BUJ, clk/2 jitter, spread-spectrum clocking (SSC)
- De-emphasis for pre- and post-cursor to emulate transmitter de-emphasis and compensate for loss in the test setup
- Inject random interference (RI) and sinusoidal interference (SI) by couplers. The M8070A software controls AWG M8195A and M8196A as RI/SI source or as aggressor lanes
- Automated jitter tolerance testing

| | NRZ  | PAM-4  |
|---|---|---|
| Effective data rate | Bit rate | Symbol rate |
| 32 Gbit/s | 32 Gb/s | 16 GBaud |
| 64 Gbit/s | 64 Gb/s | 32 GBaud |
| 128 Gbit/s | 128 Gb/s | 64 GBaud |

Covered by M8040A

| **Related IEEE802.3bs 200GBASE/200GAUI proposed symbol rate * # of lanes** | **Related IEEE802.3bs 400GBASE/400GAUI proposed symbol rate * # of lanes** | **Related OIF CEI-56G proposed symbol rates** |
|---|---|---|
| 26.5625 Gbit/s NRZ * 8 lanes | 26.5625 Gbit/s NRZ * 16 lanes | |
| 26.5625 Gbaud PAM-4 * 4 lanes | 26.5625 Gbaud PAM-4 * 8 lanes<br>53.125 Gbit/s NRZ * 8 lanes | LR-PAM-4: 19.6 to 30 Gbaud<br>MR-PAM-4: 18 to 29 Gbaud<br>MR-NRZ: 39 to 56.2 Gbit/s<br>VSR-PAM-4: 18 to 29 Gbaud<br>VSR-NRZ: 39 to 56.2 Gbit/s<br>XSR-PAM-4: 19.6 to 29 Gbaud<br>XSR-NRZ: 39.8 to 58 Gbit/s<br>USR-NRZ: 19.6 to 58.0 Gbit/s |
| | 53.125 Gbaud PAM-4 * 4 lanes | |

Figure 7. M8040A supports data rates up to 32 Gb/s NRZ, 64 Gb/s NRZ, 32 Gbaud PAM-4 and 64 Gbaud PAM-4. The user interface allows selection of NRZ and PAM-4 without reconnecting the BERT test setup.

## Master PAM-4 receiver test challenges with M8040A

Design and test engineers who need to characterize devices that support PAM-4 data formats are facing new test challenges in addition to the signal integrity issues known from 25 Gb/s NRZ device testing.

For PAM-4 input receiver tolerance test, this means impairments that may occur in the real-world should be tolerated by the receiver under test without exceeding the desired BER level. Typcial receiver tests include jitter tolerance, interference tolerance test and level sensitivity margins that are applicable for NRZ and PAM-4 devices. In addition PAM-4 receivers require additional margin testing for level non-linearity, cross-talk effects from adjacent lanes and vertical eye closure.

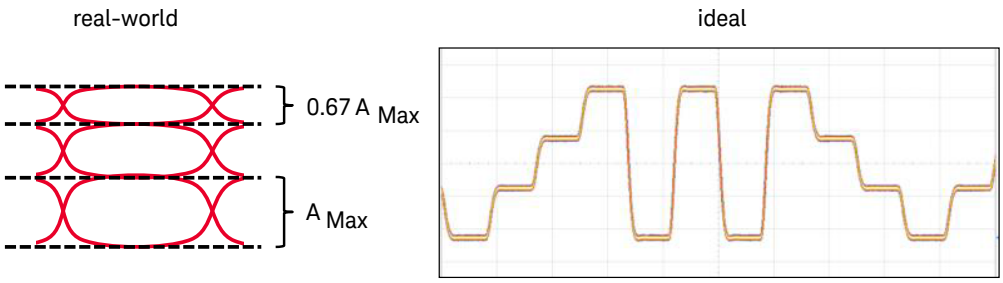
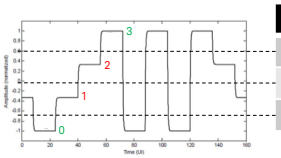



Figure 8. PAM-4 eyes can show a level separation mismatch. Receivers must be able to detect the digital signal content properly within the given mismatch ratio.

## Real-time error analysis for PAM-4 and NRZ signals

Receiver verification checks if the receiver under test operates below the specified BER while emulating the worst-case transmitter and channel conditions.
BER measurements are well established for NRZ signals by using a traditional BERT, but what does this mean for PAM-4 signals?
For proper error detection of PAM-4 signals, all thresholds ($V_{low}$, $V_{mid}$, and $V_{upper}$) have to be analyzed simultaneously to ensure a correct symbol error measurement. (See Figure 8.) If a "1" is detected at the $V_{mid}$ threshold, the received pattern can have level 2 or 3. Only if the level detected at $V_{upp}$ is checked simultaneously with $V_{mid}$, it can be determined if the received inputs have the correct level for a 2 or a 3. If two thresholds are errored within one UI, this case translates just into one symbol error.




| Detecting | 1 | 0 |
|---|---|---|
| Threshold $V_{upp}$ | = 3 | = 0 or 1 or 2? |
| Threshold $V_{mid}$ | = 2 or 3? | = 0 or 1? |
| Threshold $V_{low}$ | = 1 or 2 or 3? | = 0 |

| PAM -4 | Vupp | Vmid | Vlow | Gray | |
|---|---|---|---|---|---|
| 3 | 1 | 1 | 1 | 1 | 0 |
| 2 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 |

Figure 9. Only a true PAM-4 error analyzer like M8040A, can provide a PAM-4 symbol error rate in real-time without post-processing. Error ratios down to $10^{-15}$ or error-free can be measured even for long PRBS $2^{31}$–1, QPRBS13-CEI or QPRBS31-CEI patterns. Errored 0,1,2,3 and symbol errors can be counted separately for further debugging.

The M8040A provides real-time error analysis of PAM-4 and NRZ signals.
Key capabilities of the error analyzer module M8046A include:

- One differential channel per analyzer module
- Symbol rates from 5 to 30 Gbaud for PAM-4 and from 5 to 32 and 64 Gb/s for NRZ
- Native PAM-4 decoding
- Built-in equalization to re-open closed eyes at the analyzer input
- Selectable expected patterns like QPRBS31, pattern memory, pattern sequencing, masking, Gray coding and custom PAM-4 symbol mapping
- Clock recovery for PAM-4 and NRZ signals with N1076A and N1077A. Control via common M8000 system software
- DUT control interface allows to access built-error counters from the M8070A software

## Specifications for M8045A and M8046A modules and M8057A remote head

M8045A pattern generator module for two data channels, 3-slot AXIe


M8045A Pattern generator module for one data channel, 3-slot AXIe


M8057A remote head with cable connections (0.85 m) front and rear view

M8046A analyzer module, 1-slot AXIe


Figure 10. Front panel views of pattern generator module M8045A (top) as 2 and 1 channel (center) versions, remote head M8057A, and error analyzer module M8046A (bottom). To allow a very short connection to the device under test, the remote head is used. One remote head is needed for each of the pattern generator data outputs of M8045A.

# Specifications for pattern generator module M8045A and remote head M8057A

## Data output (DATA OUT 1, DATA OUT 2)

The pattern generator supports symbol rates up to 32 Gbaud or 64 Gbaud, default is one channel and NRZ format.
The remote head M8057A is needed once per channel. Using the P and N outputs of the M8045A without remote head is prohibited.

For the following generator functions a separate module option is required:
- PAM-4 coding up to 32 Gbaud (M8045A Option 0P3)
- PAM-4 extension to 64 Gbaud (M8045A Option 0P6)
- Second data channel (M8045A Option 0G2)
- Advanced jitter sources (M8045A Option 0G3)
- De-emphasis (M8045A Option 0G4)

Table 1. Data output characteristics for M8045A with remote head M8057A.

| **All timing parameters are measured @ 0.5 V into ground at data outputs of remote head M8057A** | |
|---|---|
| Symbol rate | 2.025 to 32.4 Gbaud for M8045A Option -G32<br>2.025 to 58.0 Gbaud (all specifications are valid up to 58 Gbaud with over-programming up to 64.8 Gbaud) for M8045A Option -G64 |
| Data format | NRZ (default)<br>PAM-4 (requires M8045A Option -0P3 and for symbol rates above 32 Gbaud -0P6 in addition) |
| Channels per module | 1 or 2 (requires M8045A Option -0G2 and second remote head) |
| Amplitude | |
| For symbol rates < 32.4 Gbaud | 50 mV to 0.9 Vpp single ended<br>100 mV to 1.8 Vpp differential |
| For symbol rates < 58 Gbaud | 50 mV to 0.6 Vpp single ended<br>100 mV to 1.2 Vpp differential |
| Amplitude accuracy | ±10% ±10 mV typical (AC) [1] |
| Output voltage window | –1 to +3.0 V |
| External termination voltage | –1 to +3.0 V. For offset > 1.3 V the termination voltage should be ± 0.5 V of offset |
| Transition time | 9 ps typical (20 to 80%) for symbol rates > 32.4 Gbaud<br>11 ps typical (20%-80%) for symbol rates ≤ 32.4 Gbaud |
| Intrinsic total jitter | 8 ps typical @ 32.0 Gb/s NRZ, PRBS 15, BER $10^{-12}$ |
| Intrinsic random jitter (NRZ) | 5 mUI rms typical @ symbol rates between 2.025 Gbaud and < 22 Gbaud<br>7 mUI rms typical @ symbol rates between 22 Gbaud and < 32.4 Gbaud<br>10 mUI rms typical @ symbol rates between 32.4 Gbaud and < 40 Gbaud<br>12 mUI rms typical @ symbol rates between 40 Gbaud and < 52 Gbaud<br>10 mUI rms typical @symbol rates between 52 Gbaud and < 58 Gbaud |
| Data delay range | 0 to 10 ns, resolution 100 fs |
| Data delay accuracy | ± ( max. (1.5 ps or 10 mUI whatever is higher) + 1% of entered value) typical [3] |
| Electrical idle | The output transitions from full swing to 0 V amplitude and vice versa at constant offset within 1 UI. |
| SNR | Tbd |
| Skew between normal and complement output | 3 ps maximum at the end of the recommended cable pair. Fixed. |
| Skew between data output ch 1 and data output ch 2 | Tbd |

1. At 5 Gbaud measured with DCA-X N1045A and clock pattern and in the middle of the eye.
2. Measured with DCA-X N1045A.
3. At constant temperature.

Table 1. Data output characteristics for M8045A with remote head M8057A. (continued)

| | |
|---|---|
| Termination impedance range | To protect the output stage, the output is disabled when an unexpected voltage or termination impedance is detected.<br>DC output coupling mode:<br>Termination range for devices connected to data out:<br>– Unbalanced 50 Ω +15 Ω / –10 Ω<br>– Typical balanced 100 Ω ±30 Ω typical<br>Operation into open is possible for these ranges when DC coupled and balanced termination modes are selected:<br>– Output amplitude max. 300 mV<br>– Offset 0 to 370 mV<br>When using AC coupled mode, an internal DC blocking capacitor is applied. |
| Termination modes | Balanced/unbalanced |
| Coupling | DC/AC selectable coupling of device under test |
| Connectors | 1.85 mm, female |

## De-emphasis (DATA OUT)

The M8045A provides built-in de-emphasis with positive and negative cursors based on a finite impulse response (FIR) filter see Figure 11. Users can enter the de-emphasis in coefficient values.

Table 2. Specifications for multi-tap de-emphasis (requires Option 0G4).

| | NRZ | PAM-4 |
|---|---|---|
| De-emphasis taps | 4, can be adjusted for each channel independently | |
| Pre-cursor coefficient c0 | 0.0 to ± 0.40 [1] | 0.0 to ± 0.40 [1] |
| Pre-cursor coefficient c1 | 0.0 to ± 0.40 [1] | 0.0 to ± 0.40 [1] |
| Main cursor coefficient c2 | 0.0 to ± 1.0 [1] | 0.0 to 1.0 [1] |
| Post-cursor coefficient c3 | 0.0 to ± 0.40 [1] | 0.0 to ± 0.40 [1] |
| Cursor coefficient resolution | 0.01 | 0.01 |

1. Sum of all cursors absolute values may not exceed 1.0 |c0| +|c1| +|c2 |+|c3| ≤ 1. Also |c0|, |c1|, |c3| < |c2|.

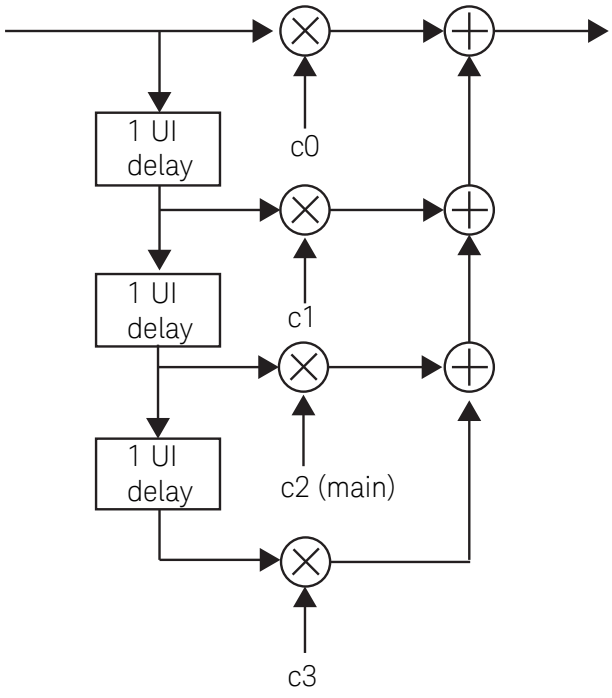



Figure 11. The pattern generator of M8045A provides integrated de-emphasis to emulate TX equalization. The post-cursor c3 , main cursor c2 and two pre cursors c0 and c1 can be adjusted.

## Clock output 1 and 2 (Channel 1 CLK OUT, Channel 2 CLK OUT)

These clock outputs provide two modes. They can operate with the same jitter as the corresponding data output or operate in a clean mode.

Table 3. Specifications for channel 1 clock output and channel 2 clock output.

| | | |
|---|---|---|
| Frequency range | | 1.0125 to 16.2 GHz with M8045A-G32<br>1.0125 to 32.4 GHz with M8045A-G64 |
| Frequency divider factors | | Symbol rate / clock divider: 2, 4, 8, 16. Divided output frequency must fit into frequency range |
| Clean clock mode | On | No jitter injection, no SSC |
| | Off | Same jitter and SSC as data output of same channel |
| Amplitude | | 1 V typical nominal single ended |
| Duty cycle | | 50%, accuracy ± 15% typical |
| Intrinsic random jitter | | 6 mUI rms typical for symbol rates between 2.025 Gbaud and ≤ 27 Gbaud<br>10 mUI rms typical for symbol rates > 27 Gbaud.<br>Refers to mUI of symbol rate. |
| Termination | | 50 Ω into GND or external termination voltage. Do not operate into open. |
| Coupling | | AC coupled |
| Connectors | | 3.5 mm, female |

## Clock output (CLK OUT)

This is a differential clock output with many sub-rate clock dividers. LF SJ and HF jitter can be turned off and on individually. HF jitter has the same setting as HF jitter of data output of channel 1.

Table 4. Clock output specifications.

| | | |
|---|---|---|
| CLK frequency range | | 1.0125 to 16.20 GHz |
| Clock divider in relation to clock frequency range | | n * (1, 2, 4, 8, 10, 16, 20, 24, 30, 32, 40, 50, 64, 66, 80) with<br>n= 1 < 16.2 GHz<br>n= 2 for 16.2 GHz to 32.4 GHz<br>n= 4 > 32.4 GHz<br>For other dividers use TRIG OUT |
| Frequency resolution | | 1 Hz |
| Frequency accuracy | | ± 15 ppm |
| Amplitude | Differential | 0.2 to 2.0 V, 10 mV steps |
| | Single ended | 0.1 to 1 V, 5 mV steps |
| Output voltage window | | –1 to +3 V [1] |
| External termination voltage | | –1 to +3 V |
| Transition times | | 20 ps typical (20 to 80%) |
| Duty cycle | | 50%, accuracy ± 15% |
| Clock modes | | See Table 5 |
| Intrinsic random jitter | | 300 fs rms typical at 16.2 GHz and clock divider = 1 |
| SSB phase noise [2] | | – 85 dBc/ Hz typical at 10 kHz offset and internal clock and 10/100 MHz as external reference clock<br>– 80 dBc/Hz with 10 kHz offset for reference clock multiplier bandwidth 0.1 MHz |
| Termination | | 50 Ω into GND or external termination voltage. Do not operate into open. Unused outputs must be terminated into termination voltage |
| Coupling | | DC coupled, differential |
| Connectors | | 3.5 mm, female |

1. If $V_{term}$ is other than 0 V the following applies:
   High level voltage range= 2/3 * $V_{term}$ – 0.95 V < HIL < $V_{term}$ + 2 V
   Low level voltage range= 2/3 * $V_{term}$ – 1 V < LOL < $V_{term}$ + 1.95 V
2. For 8.1 to 16.2 GHz clocks.

Table 5. Clock modes.

| Clock mode | Clock generation | Input frequency range |
|---|---|---|
| Internal | PLL with internal reference | N/A |
| Reference | PLL with bandwidth below 1 kHz | 10/100 MHz |
| Direct | No PLL. Maximum symbol rate is 16.2 Gbaud | 8.1 to 16.2 GHz |
| Reference clock multiplier bandwidth 100 kHz | m/n PLL with loop bandwidth 100 kHz<br>m, n = 1 to 1620 | 10 MHz to 16.2 GHz |

# Supplementary inputs and outputs of M8045A

## Reference clock input (REF CLK IN)

This input allows locking the system clock to an external reference clock of 10 or 100 MHz instead of the internal oscillator. It also allows using an external clock, see clock modes as shown in table 5. A SSC tolerant PLL is used to multiply the external reference clock to the system clock.

Table 6. Reference clock input specifications (M8045A only).

| | |
|---|---|
| Input amplitude | 0.2 to 1.4 Vpp |
| Input frequency | 10 MHz to 16.2 GHz, depends on clock mode and max. data rate option |
| Interface | Single ended. 50 Ω nominal |
| Connector | SMA, female |

## Trigger output (TRG OUT)

This output is used to send a trigger signal to another connected device, such as an oscilloscope. Also it can be used to generate a subrate clock.

The trigger output can be used in different modes:

1. Divided clock, dividers:
   a. For < 16.2 Gbaud trigger data rate range 2 to 65532
   b. For 16.2 to 32.4 Gbaud trigger data rate range 4 to 65532 with step resolution of 2
   c. For > 32.4 Gbaud trigger output data rate range 8 to 65532 with step resolution of 4
2. Sequence block trigger with adjustable pulse width and offset
3. PRBS sequence trigger with adjustable pulse width

Table 7. Trigger output specifications.

| | | |
|---|---|---|
| Amplitude | single-ended | 0.1 to 1.0 Vpp |
| | differential | 0.2 to 2.0 Vpp |
| Output voltage window | | –1 to 3 V [1] |
| External termination voltage | | –1 to 3 V |
| Interface | | Differential, 50 Ω |
| Connector | | 3.5 mm, female |

1. If $V_{term}$ is other than 0 V the following applies:
   High level voltage range= $2/3*V_{term}$ – 0.95 V < HIL < $V_{term}$ + 2 V
   Low level voltage range= $2/3*V_{term}$ – 1 V < LOL < $V_{term}$ + 1.95 V

## Reference clock output (REF CLK OUT)

Outputs a 10 and 100 MHz clock, 1 Vpp single ended into 50 Ω.
Connector: SMA, female.

## Control input A and B (CTRL IN A, CTRL IN B)

Functionality of each input can be selected as: sequence trigger, error add and pattern capture event.

Table 8. Control input specifications.

| | |
|---|---|
| Input voltage | –1 V to +3 V |
| Termination voltage | –1 V to +3 V |
| Threshold voltage | –1 V to +3 V |
| Delay to data output | < 1 ms |
| Connector | 3.5 mm, female |

# Supplementary inputs and outputs of M8045A (continued)

## Control output A and B (CTRL OUT A, CTRL OUT B)

Generates a pulse or static high/low if used from sequencer.

Table 9. Control output specifications.

| | |
|---|---|
| Amplitude [1] | 0.1 to 2 V |
| Output voltage [1] | –0.5 to 1.75 V |
| Delay to data output | ±512 UI ± jitter amplitude/2 (requires M8070A software 4.0 or later) |
| Connector | 3.5 mm, female |

1. When terminated with 50 Ω into GND. Doubles into open.

## Synchronization out (SYNC OUT)

The sync output is a clock output to synchronize additional modules to a common clock. Can be used to sync the M8046A with the system internal clock.

## System input A/B (SYS IN A/B)

These are control inputs to synchronize events for the pattern sequencer.

Table 10. System input specifications.

| | |
|---|---|
| Input voltage | –1 V to +3 V |
| Termination voltage | –1 V to +3 V |
| Threshold voltage | –1 V to +3 V |
| Delay to data output | Tbd [1] |
| Connector | SMA, female |

1. Contact factory for availability. Free software upgrade.

## System output A/B (SYS OUT A/B)

Generates a pulse or static high/low controlled by the pattern sequencer. A and B outputs are independently controllable.

Table 11. System output specifications.

| | |
|---|---|
| Amplitude [1] | 0.1 to 2 V |
| Output voltage [1] | –0.5 to 1.75 V |
| Delay to data output | ±512 UI ± jitter amplitude /2 (requires M8070A software 4.0 or later) |
| Connector | SMA, female |

1. When terminated with 50 Ω into GND. Doubles into open.

## Auxiliary input (AUX IN)

Not used.

## Clock input (CLK IN)

For future use. See reference clock input for direct clock mode.

# Jitter specifications

The M8045A has integrated and calibrated jitter sources. To use the jitter injection the M8045A Option –0G3 is required.

Table 12. Specifications for low frequency periodic jitter (requires Option -0G3 advanced jitter sources).

| | | |
|---|---|---|
| Low frequency periodic jitter (LF PJ)<br><br>(generated by IQ modulator) | Amplitude range | 0 to 123.5 UI * symbol rate (in Gbaud) for modulation frequencies of 100 Hz to 10 kHz, see table below. For modulation frequencies between 10 kHz and 40 MHz the maximum<br><br>$\text{LF PJ} = \frac{7.792\ \text{UI} * 10^{-3} * \text{symbol rate}}{\text{modulation frequency}^{1.2}}$ |
| | Frequency | 100 Hz to 40 MHz, sinusoidal modulation |
| | Jitter amplitude accuracy | ±2% ± 1 ps typical |
| | Adjustable | For each data channel independently, same LFPJ for clock and trigger |

## Low frequency periodic jitter

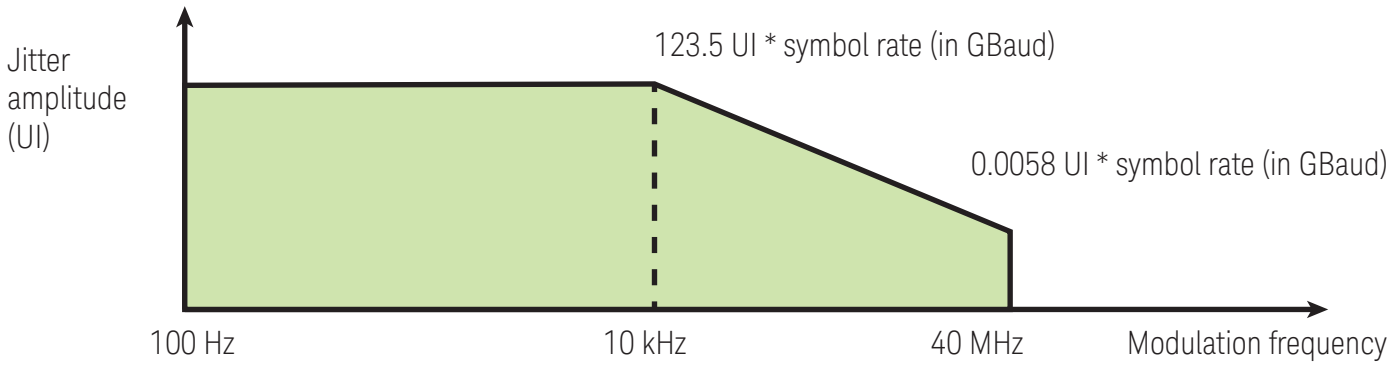



Figure 12. Low frequency periodic jitter maximum depends on data rate and modulation frequency.

Table 13. Low frequency periodic jitter ranges.

| Symbol rate | Max UI at modulation frequency 100 Hz to 10 kHz | Max UI at modulation frequency 10 MHz | Max UI at modulation frequency 40 MHz |
|---|---|---|---|
| 2.025 to 4.05 Gbaud | 250 to 500 UI | 0.0625 to 0.125 UI | 0.012 to 0.024 UI |
| 4.05 to 8.1 Gbaud | 500 to 1000 UI | 0.125 to 0.25 UI | 0.024 to 0.048 UI |
| 8.1 to 16.2 Gbaud | 1000 to 2000 UI | 0.25 to 0.5 UI | 0.048 to 0.095 UI |
| 16.2 to 32.4 Gbaud | 2000 to 4000 UI | 0.5 to 1 UI | 0.095 to 0.19 UI |
| 32.4 to 64.8 Gbaud | 4000 to 8000 UI | 1 to 2 UI | 0.19 to 0.38 UI |

Table 14. Specifications for high frequency periodic jitter, random jitter, bounded uncorrelated jitter, clock /2 jitter (all require M8045A Option -0G3 advanced jitter sources).

| | | |
|---|---|---|
| High frequency jitter (generated by delay line) | Range | 1 UI for > 32.4 Gbaud,<br>for ≤ 32.4 Gbaud minimum of:<br>- 1 UI<br>- 1 UI - (PJ frequency - 250 MHz) / 100 MHz * 0.2 UI<br>- 0.5 UI if RJ low pass filter is 1000 MHz<br>- 0.5 UI if external delay modulation is on<br>Note: This is max sum of RJ, HF-PJ1 and HF-PJ, external delay modulation and BUJ. |
| High frequency periodic jitter (HF PJ1 and HF PJ2) | Range | See HF jitter above [1] |
| | Frequency | 1 kHz to 500 MHz. For symbol rates<br>< 4 Gbaud the max modulation frequency is symbol rate / 8.<br>Two tone possible. Sweep. |
| | Jitter amplitude accuracy | ±3 ps ± 10% typical [2] |
| | Adjustable | For each channel independently |
| Random jitter (RJ) | Range | 0 to 72 mUI rms (1 UI p-p max.) [1] |
| | Jitter amplitude accuracy | ±300 fs ± 10% typical |
| | Filters | High-pass: 10 MHz and "off",<br>Low-pass: 100 MHz,<br>Low pass: 500 MHz (for symbol rates ≥ 3.75 Gbaud),<br>Low pass: 1 GHz (for symbol rates ≥ 7.5 Gbaud) |
| | Adjustable | For each channel independently |
| | Crest factor | 14 (peak-peak to rms ratio) |
| Bounded uncorrelated jitter (BUJ) | Range | See HF jitter above [1] |
| | PRBS polynomials | $2^n$–1, n = 7, 8, 9, 10, 11, 15, 23, 31 |
| | Filters | 50/100/200 MHz low pass 3rd order |
| | Jitter amplitude accuracy | ± 5 ps ± 10% typical for settings shown in Table 15 |
| | Adjustable | For each channel independently |
| | Rate for PRBS generator | 625 Mb/s, 1.25 Gb/s, and 2.5 Gb/s |
| Clock/2 jitter | Range | ± 100 mUI or ±5 ps typical (whatever is less). Note: this means that first eye can be up to 100 mUI or 5 ps longer or shorter than subsequent eye. |
| | Adjustable | For each channel independently |

1. Range of HF jitter applies to sum of RJ, HF-PJ1 and HF-PJ2, external delay modulation and BUJ.
2. For symbol rates above 32.4 Gbaud at an ambient temperature of 25 ± 6 °C

Table 15. BUJ accuracy applies for these BUJ settings.

| **BUJ calibration settings [1]** | **Rate for PRBS generator** | **PRBS polynomial** | **Low pass filter** |
|---|---|---|---|
| CEI 6G | 1.25 Gb/s | PRBS $2^9$–1 | 100 MHz |
| CEI 11G | 2.5 Gb/s | PRBS $2^{11}$–1 | 200 MHz |
| Gaussian | 2.5 Gb/s | PRBS $2^{31}$–1 | 100 MHz |
| CEI 25G | 2.5 Gb/s | PRBS $2^{11}$–1 | 200 MHz |
| CEI 56G | 2.5 Gb/s | PRBS $2^{11}$–1 | 200 MHz |

1. Other settings are not calibrated and do not necessarily generate the desired jitter histograms for all data rates of the PRBS generator.

Table 16. Specifications for spread spectrum clocking (SSC). Requires M8045A Option -0G3 advanced jitter sources.

| | | |
|---|---|---|
| SSC (spread spectrum clock) | Symbol rate range for SSC | 2.025 to 32.4 Gbaud |
| | Range | 0 to 10,000 ppm (0 to 1%) peak-peak. Select center-spread, up-spread, and down-spread. |
| | Frequency | 100 Hz to 200 kHz |
| | Modulation | Triangular and arbitrary modulation |
| | SSC amplitude accuracy | ±0.025% typical |
| | Outputs | Can be turned on/off together for CLK OUT, DATA OUT 1, DATA OUT 2, TRG OUT, CLK OUT channel 1/2 |

## External jitter modulation

An external modulation source can be used to modulate the delay of the M8045A data outputs, clock output and trigger output.

## DATA MOD IN 1, 2

This input can be used for delay modulation by an external source for each data output channel individually.

Table 17. Specifications for external jitter modulation on data outputs.

| | | |
|---|---|---|
| External jitter - data modulation input 1 and 2 | Range | Up to 1 UI for symbol rates > 32.4 GBaud<br>Up to 0.5 UI for symbol rates ≤ 32.4 GBaud [1]<br>0.8 Vpp max |
| | Frequency | Up to 500 MHz |
| Gain | | 1UI/0.725 V ± 5% typical [2] |
| Linearity | | 50 mUI |
| Connectors | | 3.5 mm, female |

1. See HF jitter specifications for the maximum sum of RJ, HF-PJ1 and HF-PJ2 external delay modulation and BUJ.
2. For symbol rates above 32.4 Gbaud at an ambient temperature of 25 ± 6 °C

## CLK MOD IN

This input can be used for delay modulation of TRIG OUT and CLK OUT, the modulation always affects both outputs.

Table 18. Specifications for external jitter modulation for clock and trigger.

| | | |
|---|---|---|
| External jitter - clock modulation input | Description | Input for the delay modulation for the TRG OUT and CLK OUT. Affects both |
| | Range | Up to 1 UI for symbol rates > 32.4 Gbaud<br>Up to 0.5 UI for symbol rates ≤ 32.4 Gbaud [1]<br>0.8 Vpp max |
| | Frequency | Up to 500 MHz |
| Gain | | 1UI/0.725 V ± 5% typical [2] |
| Linearity | | 50 mUI |
| Connectors | | SMA, female |

1. See HF jitter specification for the maximum sum of RJ, HF-PJ1 and HF-PJ2, external delay modulation and BUJ.
2. For symbol rates above 32.4 Gbaud at an ambient temperature of 25 ± 6 °C

## External level interference (RI/SI) sources

The Keysight M8195A and M8196A AWG can be used as level interference source with sinusoidal and random modulation. The M8070A system software controls the interference parameters such as amplitude, bandwidth, crest factor. Keysight provides a matched directional coupler pair for injecting the RI or SI signal before or after the channel. See table below.

Table 19. Specifications for external level interference sources RI/SI with M8195A, M8196A

| | M8070A parameters | M8195A | M8196A |
|---|---|---|---|
| Random Interference (RI) | | Yes | Yes |
| | Amplitude range (single ended, at DAC output of AWG) | 80 mV to 1 V | 80 mV to 1 V |
| | Lowest frequency range | 320 kHz -20 GHz (ch1 with deep memory: 100 Hz to 25 GHz) | 160 kHz to 32 GHz |
| | Highest frequency range | 320 kHz to 25 GHz | 160 kHz to 32 GHz |
| | Crest factor (peak ratio) | Tbd | Tbd |
| Sinusoidal interference (SI) | | Yes | Yes |
| | Amplitude range (single ended, at DAC output of AWG) | 80 mV to 1 V | 80 mV to 1 V |
| | Lowest frequency range | 320 kHz -20 GHz (ch1 with deep memory: 100 Hz to 25 GHz) | 160 kHz to 32 GHz |
| Recommended accessories | M8045-802 Matched directional coupler pair, 50 GHz, 13 dB, 2.4 mm | | |
| Software pre-requisites | M8070A software 3.4 or higher | M8195A firmware V3.2.0 or higher | M8196A firmware V2.0.39 or higher |

# Pattern and sequencer

Table 20. Specifications for pattern, sequencer.

| | |
|---|---|
| PRBS [1] | $2^n$–1, n= 7, 10, 11, 15, 23, 23p, 31, 33, 35, 39, 45, 49, 51, 58 |
| PRBS | $2^n$, n = 7, 10, 11, 13, 15, 23 |
| QPRBS | OIF-CEI: QPRBS13-CEI, QPRBS31-CEI<br>IEEE 802.3: QPRBS13, PRBS13Q, PRBS31Q, SSPRQ |
| New patterns in library | PAM-4-linearity, JP03A, JP03B |
| PAM-4 coding | Gray coding, custom mapping of 00, 01,10,11 to symbols 0,1,2,3 |
| Mark density | PRBS 1/8 to 7/8 |
| Zero substitution | Yes |
| Export/Import | Patterns from M8000 and N4900 series can be imported |
| Pattern library | Yes |
| User definable memory | NRZ: 2 Gbit/channel<br>PAM-4: 1 Gsymbol/channel |
| Vector/sequence granularity | 512 bit |
| Pattern capture | Yes, raw data for PAM-4<br>Capture data starts on event<br>– User defined (minimum) amount of pre-event bits/ symbols and minimum capture bit/symbols<br>– Events: error, CTRL IN A /B, immediate<br>– Max 2 Gbit/ch capture data for NRZ, 1 Gsymbol/ch for PAM-4<br>Save captured data:<br>– With errors<br>– As expected data (ignores error content)<br>– As PG data (ignores error content)<br>– Export via pattern editor windows<br>– Convert bits into all other codings and vice versa<br>– Ability to mask error bits automatically<br>Display of captured data:<br>– Display errors with color coding<br>Navigate through error bits/symbols (find next/previous) |
| Pattern sequencer | 3 counted loop levels, 1 infinite loop, # of blocks: 500 |
| Masking | Expected bits and be masked (ignored) during error counting. Bitwise and block-wise masking is possible. |

1. Polarity is inverted compared to ParBERT and J-BERT N4903A/B and N49xx series.
2. M8045A only

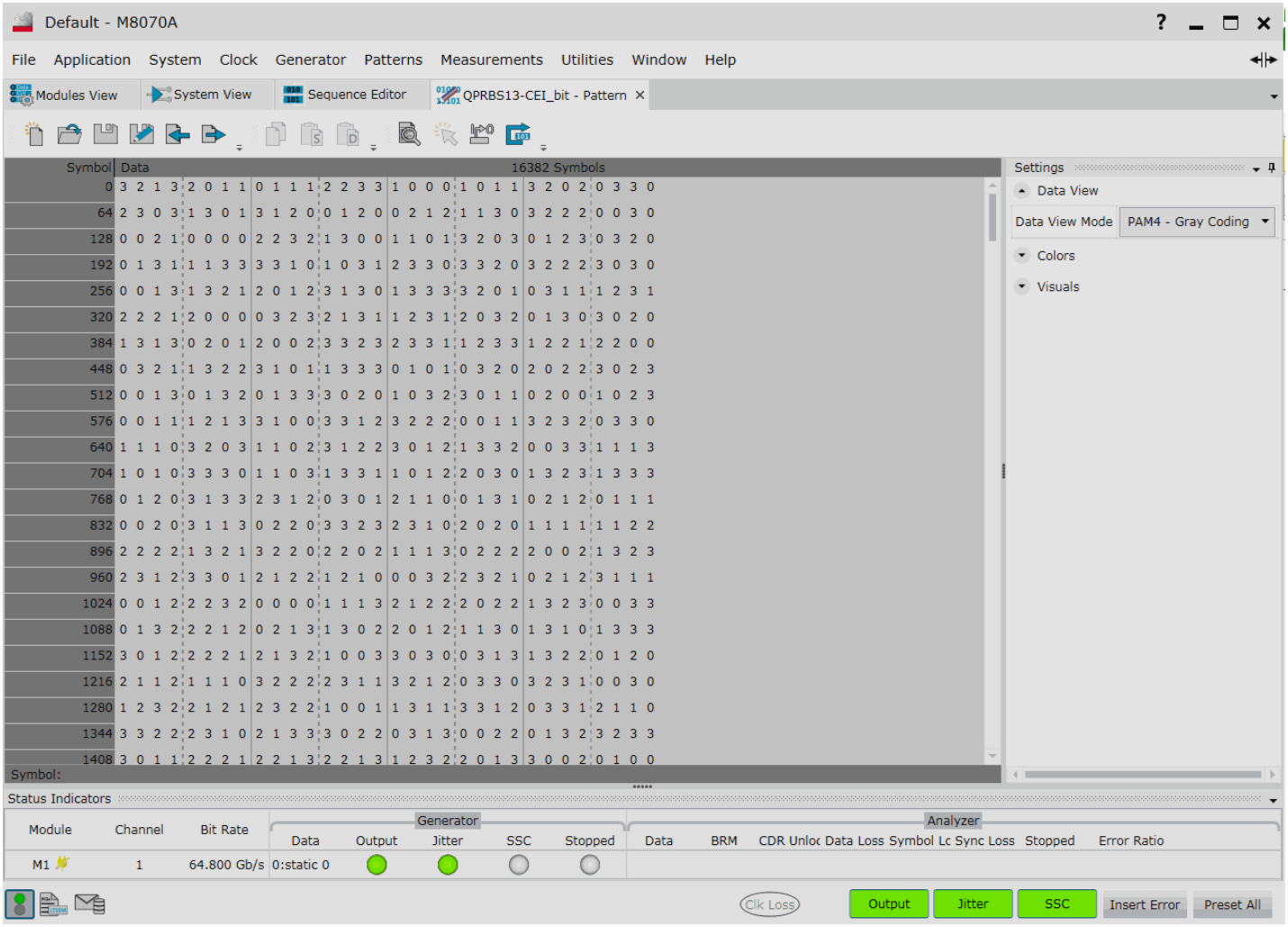



Figure 13. The pattern editor in the M8070A software allows editing NRZ bits and PAM-4 symbols. The PAM-4 symbol to bit mapping can be selected as Gray coded or custom with adjustable PAM-4 levels. Quaternary PRBS, like QPRBS13-CEI or QPRBS31, according to CEI and IEEE standards can be selected as well as SSPRQ and PAM-4 linearity test patterns.

# Specifications analyzer module (error detector) M8046A


Figure 14. Front panel of M8046A

The M8046A supports symbol rates up to 32 Gbaud, and 64 Gbaud, the default is 32 Gbaud and NRZ format.
The analyzer module can be used for error analysis in conjunction with the M8045A pattern generator and the M8195A/M8196A arbitrary waveform generator. For the following functions a separate module option is required:

- PAM-4 decoding up to 32 Gbaud (M8046A Option -0P3)
- Equalization for symbol rates above 32.4 Gbaud (M8046A Option -0A3)

## Data input (DATA IN)

Table 21. Specifications for analyzer/error detector.

| | |
|---|---|
| Symbol rate | 5.0 to 32.4 Gbaud NRZ for M8046A-A32<br>5.0 to 30 Gbaud PAM-4 for M8046A-A32 with -0P3<br>*5.0 to 64.8 Gbaud NRZ for M8046A-A64 (preliminary)* |
| Channels per module | 1 |
| Data format | NRZ (default)<br>PAM-4 (requires M8046A Option -0P3) |
| Max # of M8046A per M9505A chassis | up to 4 |
| Input sensitivity [1] | NRZ: 70 mV single ended and differential<br>PAM-4: 70 mV per eye single ended and differential |
| Max input voltage amplitude | 1000 mVpp differential |
| Input voltage window | -1 V to +3 V |
| Timing resolution | 0.1 ps |
| Input bandwidth | 16 GHz typical |
| Sampling point | Manual and automatic. Finds optimum voltage range, threshold and delay of the sampling point.<br>Delay accuracy is 20 mUI or 1.5 ps whichever is higher.<br>One sampling edge per UI. |
| Decision threshold range | Full input voltage range with 1 mV resolution |
| Input equalizer [3] | *Up to 13 dB at 32.4 Gbaud NRZ*<br>*Up to 5 dB at 30 Gbaud PAM-4*<br>*Up to 4 dB at 26.5625 Gbaud PAM-4*<br>*FFE with 15 presets*<br>*For symbol rates above 32 Gbaud:*<br>*Up to 3 dB at 58 Gb/s for NRZ signals. (requires M8046A-0A3 and -A64)* |
| Phase margin [2] NRZ | 1 UI – 12 ps typical for PRBS $2^{15}$– 1<br>1 UI – 8 ps typical for clock pattern |
| PAM-4 | 1 UI – 34 ps typical for PRBS $2^{15}$– 1 |
| Interface | Differential: 100 Ω,<br>Single ended: 50 Ω<br>AC coupled, terminate unused input with 50 Ω |
| Connectors | 2.4 mm, female |

1. Measured with PRBS $2^{31}$ – 1 at 32.4 Gb/s NRZ or 30 Gbaud PAM-4, at BER of $10^{-12}$.
2. Measured at 26.5625 Gbaud and BER of $10^{-12}$.
3. Preliminary specifications. Requires M8070A software 3.7 or higher. The preset characteristic can vary by module hardware and symbol rate and might change with a future software revision. Valid at input of the reference cable for M8046A.

## External clock input (CLK IN)

Table 22. Specifications for clock input of analyzer.

| | |
|---|---|
| Amplitude | Minimum 200 mVpp, maximum 1 Vpp |
| Frequency range [1] | 2.5 to 32.4 GHz<br>Note: In clk "x 2" mode for symbol rates above 25 Gbaud an external bandpass filter (M8061A-803) has to be used on the clock input. The filter has to be removed for symbol rates below 25 Gbaud.<br>In clk "x 1" mode no filter is needed. |
| Multiplier internal | 1, 2 |
| Connector | 3.5 mm, female |

1. below 5 GHz transition time of clock signal should be < 25 ps.

## SYNC input (SYNC IN)

Can be used to clock the analyzer from the pattern generator's M8045A system clock via the sync output A/B (requires cable M8051A-801). Not needed if external clock is used.

## Control input A (CTRL IN A)

Functionality can be selected as: sequence trigger, pattern capture event.

Table 23. Specifications for control inputs of analyzer.

| | |
|---|---|
| Input voltage | –1 to +3 V |
| Termination voltage | –1 to +3 V |
| Threshold voltage | –1 to +3 V |
| Response time | ± 512 UI repeatability |
| Connector | 3.5 mm, female |

## Control output (CTRL OUT A)

Outputs a pulse in case of an error. Generates a pulse or static high/low if used from sequencer.

Table 24. Control output specifications for M8046A.

| | |
|---|---|
| Amplitude | 0.1 to 2 V |
| Output voltage | –0.5 to 1.75 V |
| Delay from data input | Tbd |
| Response time | Tbd |
| Connector | 3.5 mm, female |

# Measurements

Table 25. Measurement capabilities.

| | |
|---|---|
| BER, SER | Accumulation and instantaneous |
| Jitter tolerance | Yes |
| BERT Scan with RJ, DJ separation | No [2] |
| Output level and Q-factor | No |
| Counters | Compared bits, errored bits<br>Compared 0 bits, errored 0 bits<br>Compared 1 bits, errored 1 bits<br>Compared symbols, errored symbols<br>Compared symbols 0, 1, 2, 3<br>Errored symbols 0, 1, 2, 3 |
| BER versus parameter automated sweep | Yes |
| Burst error analysis [1] | Yes [1] |

1. Contact factory for availability.
2. The measurement is available in the user interface, but just for debugging/troubleshooting purposes. The accuracy of jitter separation results is unspecified in case of NRZ and invalid in case of PAM-4 signals.

## Clock recovery

The Keysight N1076A and N1077A clock recovery units can be used to recover a clock from NRZ and PAM-4 patterns to clock the M8046A error analyzer. The clock recovery units can be controlled from the M8070A system software for BER and jitter tolerance testing.

The N1076A and N1077A clock recovery unit can be used with M8046A as external clock recovery. They can be controlled from the M8070A system software. Offline mode is supported.

Table 26. Conditions for use of external clock recovery.

| | |
|---|---|
| Symbol rate | 5.0 to 32.4 GBaud |
| Sensitivity<br>(with recommended accessories) | NRZ: 200 mV<br>PAM-4: 360 mV (120 mV per eye)<br>Single ended and differential |
| Number of consecutive bits without transition | NRZ: 144<br>PAM-4: 77 |
| Measurememnts | Jitter tolerance, BER |
| Software pre-requisites | M8070A 3.6 or higher<br>N1010A Flex DCA A.05.61 or higher, no extra licenses needed<br>Note: The M8070A and the N1010A controlling the N1076A/77A should run on the same controller. The N1010A Flex DCA software cannot be operated interactively while being controlled by M8070A. If a DCA-M has to be used in the same test setup, we recommend to control it from a second PC/controller. |
| Hardware pre-requisites | M8046A with serial number >DE56800200<br>(pre-release units have to be upgraded to 32 Gbaud release status)<br>N1076A-232 or N1077A-232 for symbol rates above 16 Gbaud |
| Recommended accessories<br>(for differential signals) | – Qty 1 of Keysight N1027A-2P2 microwave pick-off tee, 2.4 mm connectors, matched pair<br>– Qty 2 of Keysight 11900B adapter 2.4 mm (f) to 2.4 mm (f) for connecting with M8046A data input reference cable pair<br>– Qty 2 of Keysight 83059A adapter 3.5 mm (m) to 3.5 mm (m) for mounting the pick-off tee directly to inputs of N1076A/77A<br>– M8046A-802 matched cable pair 2.4 mm, 2 ps for data inputs of M8046A |

# User interface and remote control

The M8070A system software for the M8000 Series of BER test solutions is required to control the M8040A BERT.

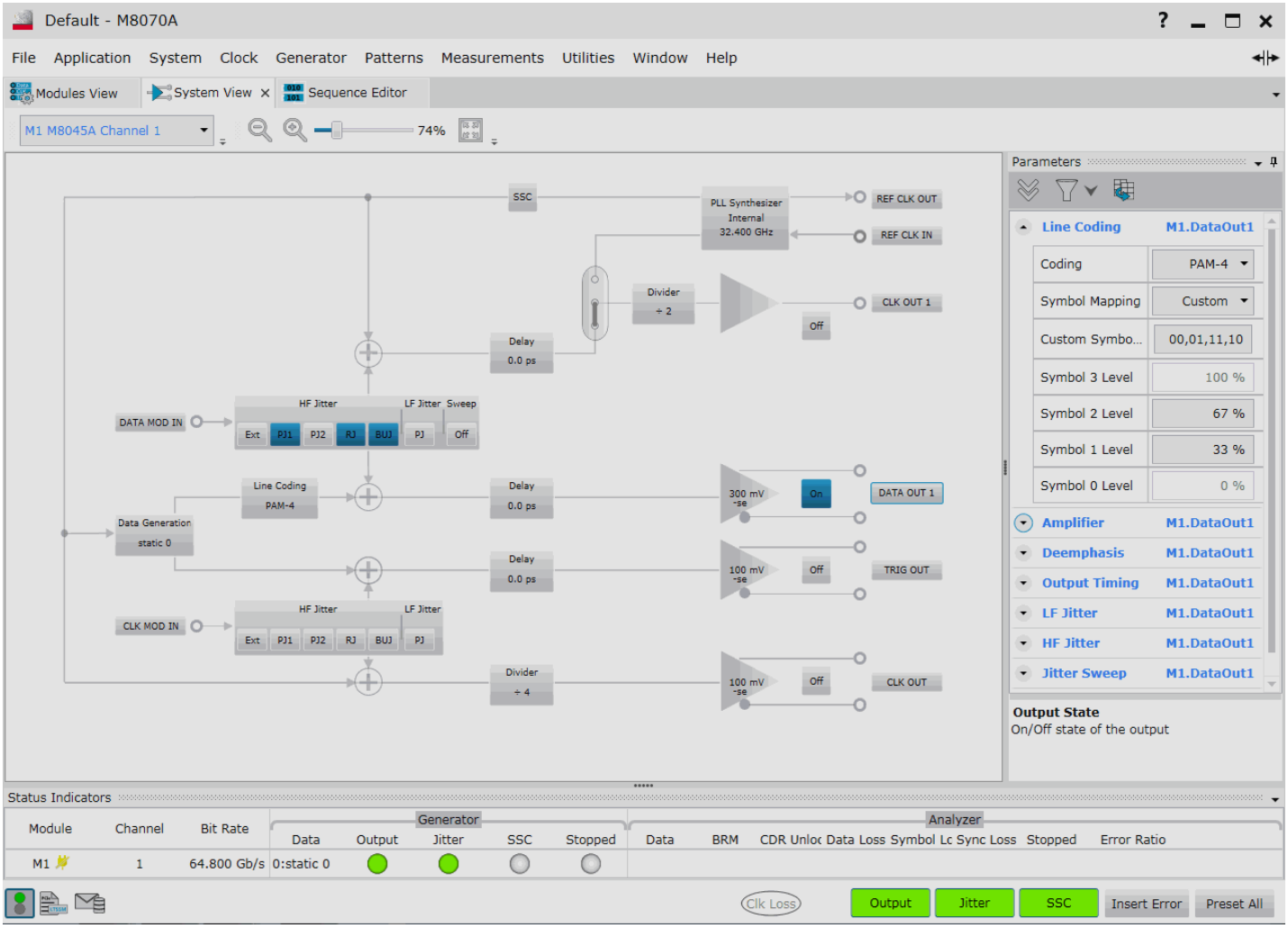



Figure 15. The graphical user interface offers multiple views that can be defined by the user. This example shows the preliminary system view on the left side and the pattern generator data output with the PAM-4 coding and level linearity parameters at the right.

Table 27. User interface and remote control interface.

| System software | M8070A |
|---|---|
| Software licensing | Offline version does not require a license. For controlling the hardware you can choose between a transportable, perpetual license (M8070A-0TP) and a network, perpetual license (M8070A-0NP). The network license is only recommended when using multiple M8040A setups within one company. When ordering M8040A-BU1 the M8070A-0TP license will be pre-installed on the embedded controller. |
| Controller requirements | Embedded PC: Choose M8040A-BU1 for a pre-installed embedded controller M9537A including pre-installation of M8070A software and module licenses. Otherwise: M9537A 1-slot AXIe embedded controller, choose options for Windows 7, 8 or 10, 8 or 16 GB RAM, SSD.<br>External PC: USB connection recommended between external PC and AXIe chassis. Minimum of 8 GB RAM recommended. For PCIe connectivity please refer to list of tested PCs for AXIe Technical Note, pub no. 5990-7632EN |
| Operating system | Microsoft Windows 7 (64 bit) SP1, Windows 8 (64 bit), Windows 8.1 (64 bit), Windows 10 |
| Controller connectivity with AXIe chassis | USB 2.0 (Mini-B) recommended, PCIe 2.0/8x (only for highest data throughput and desktop PC) |
| Programming language | SCPI. Not compatible with N4900 Series and ParBERT 81250A |
| Remote control interface | Desktop or Laptop PC: LAN<br>M9537A: LAN |
| Save/Recall | Yes |
| Export of measurement results | Jitter tolerance results as *.csv file |
| Display resolution | Minimum requirement 1024 x 768 |
| Scripting interface | The built-in scripting engine is based on IronPython.<br>It enables the control of the device under test as well as other test equipment.<br>Function hooks are available to tailor your measurements, such as read-out of built-in error counters or initializing the device |
| DUT control interface | Enables access to built-in error counters and status registers of a device under test (BIST) for use with automated measurements like accumulated BER and jitter tolerance. Can also be used to customize the measurements to DUT specific needs. IronPython scripting and .net libraries are supported to interface with the DUT. Requires option M8070A-1TP or -1NP |
| Software pre-requisites | Microsoft Win 7 SP1 or 8 / 8.1, 10, Keysight IO library rev. 17.2.20605 or above |
| Software download | See http://www.keysight.com/find/m8070a for latest version<br>Minimum software required to control M8040A is M8070A revision 3.5.1 or higher |

# General characteristics and physical dimensions

## Modules M8045A and M8046A

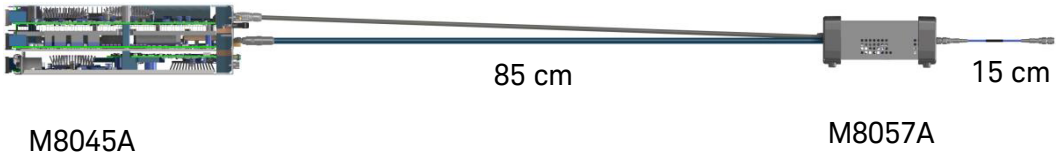
Table 28. General characteristics for M8045A and M8046A modules.

| | M8045A | M8046A |
|---|---|---|
| Operating temperature | 5 to 40 °C (41 to + 104 °F) | |
| Storage temperature | –40 to +70 °C (modules) (–40 to + 158 °F) | |
| Operating humidity | 15 to 95% relative humidity at 40°C (non-condensing) | |
| Storage humidity | 24 to 90% relative humidity at 65°C (non-condensing) | |
| Power requirements (module only) | Single channel: 515 W<br>Dual channel: 605 W | 238 W |
| Physical dimensions for modules<br>(W x H x D) | 3-slot AXIe module:<br>351 x 92 x 315 mm<br>(13.8 x 3.6 x 12.4 inch) | 1-slot AXIe module:<br>351 x 30 x 309 mm<br>(13.8 x 1.8 x 12.2 inch) |
| Physical dimensions for M8040A-BU1/-BU2<br>(W x H x D) | Installed in 5-slot AXIe chassis:<br>462 x 193 x 446 mm (18.2 x 7.6 x 17.6 inch) | |
| Weight net | M8045A module: single channel 6.9 kg (15.2 lb)<br>M8045A dual channel: 7.5 kg (16.5 lb)<br>With M8040A-BU1: 25 kg (55 lb)<br>With M8040A-BU2: 21 kg (46.3 lb) | M8046A module: 3.6 kg (8.0 lb)<br><br>In bundle with M8045A and in a 5-slot chassis:<br>24.6 kg (54.3 lb) |
| Weight shipping | M8045A module: 11 kg (24 lb)<br>With M8040A-BU1: 37 kg (82 lb)<br>With M8040A-BU2: 33 kg (73 lb) | M8046A module: 7.5 kg (16 lb)<br>In bundle with M8045A and in a 5-slot chassis:<br>37.6 kg (83 lb) |
| Recommended recalibration period | 1 year | |
| Warm-up time | 30 minutes | |
| Cooling requirements | Slot air flow direction is from right to left. When operating the M8045A /46A choose a location that provides at least 50 mm of clearance at each side. See also start-up guide for M9505A chassis. | |
| EMC | IEC 61326-1 | |
| Safety | IEC 61010-1 | |
| Quality management | ISO 9001, 14001 | |

## Remote head M8057A

Table 29. General characteristics for M8057A remote head.

| | **M8057A** |
|---|---|
| Operating temperature | 5 to 40 °C (41 to + 104 °F) |
| Storage temperature | –40 to +70 °C (modules) (–40 to + 158 °F) |
| Operating humidity | 15 to 95% relative humidity at 40 °C (non-condensing) |
| Storage humidity | 24 to 90% relative humidity at 65 °C (non-condensing) |
| Physical dimensions (W x H x D) | Remote head 117 mm x 68 mm x 185 mm, (4.6” x 2.7” x 7.3”) |
| Physical dimensions for remote head with cable | Length of cable connection between M8057A and M8045A module: 85 cm |




| | |
|---|---|
| Weight net | 1.7 kg (3.75 lb) |
| Weight shipping | 6.5 kg (14.4 lb) |
| Recommended recalibration period | 1 year |
| Warm-up time | 30 minutes |
| EMC | IEC 61326-1 |
| Quality management | ISO 9001, 14001 |

# Specification assumptions

The specifications in this document describe the instruments' warranted performance. All specification in this revision of the data sheet are preliminary. Non-warranted values are described as typical. All specifications are valid in the specified operating temperature range after the warm-up time and after auto-adjustment. If not otherwise stated all outputs need to be terminated with 50 Ω to GND. All M8045A specifications if not otherwise stated are valid at the end of the cable M8045A-801.

All M8046A specifications if not otherwise stated are valid using the recommended cable pair M8046A-802 (2.4 mm matched cable pair). Preliminary specifications are written in italics.

# Ordering of M8040A High-performance BERT 64 Gbaud

The M8040A is scalable and upgradeable. The following table shows all available options. Upgrade options are shown below.

| Description | Product # | Option | Comment |
|---|---|---|---|
| High-performance BERT 64 Gbaud (systemizing number for factory pre-installation) | M8040A | | |
| **Pattern generator and clock module, 32/64 Gbaud, 3-slot AXIe** | **M8045A** | | |
| Pattern generator one channel NRZ, data rate up to 32 Gbaud (requires remote head, M8057A) | M8045A | G32 | One of these is required |
| Pattern generator one channel NRZ, data rate up to 64 Gbaud (requires remote head, M8057A) | M8045A | G64 | |
| Second channel, hardware and license (requires remote head, M8057A) | M8045A | 0G2 | |
| Advanced jitter sources for receiver characterization, module-wide license | M8045A | 0G3 | |
| De-emphasis, module-wide license | M8045A | 0G4 | |
| PAM-4 encoding up to 32 Gbaud, module-wide license | M8045A | 0P3 | |
| Extension to PAM-4 encoding up to 64 Gbaud, module-wide license | M8045A | 0P6 | Only with G64 |
| Short cable 1.85 mm (m) to 1.85 mm (m), 0.15 m, absolute matching 699 ps ± 1 ps | M8045A | 801 | Qty 2 recommeded |
| Remote head for M8045A pattern generator, 1 channel | M8057A | | |
| **Analyzer module, 32/64 Gbaud, 1-slot AXIe** | **M8046A** | | |
| Analyzer, one channel, data rate up to 32 Gbaud, NRZ | M8046A | A32 | |
| Analyzer, one channel, data rate up to 64 Gbaud, NRZ | M8046A | A64 | |
| Equalization, license | M8046A | 0A3 | Only with A64 |
| PAM-4 decoding up to 32 Gbaud, license | M8046A | 0P3 | |
| Cable 2.92 mm (m) to 2.92 mm (m), 0.5 m for clock input | M8046A | 801 | Qty 1 recommended |
| **Software and chassis** | | | |
| System software for M8000 Series (transportable perpetual or network license) | M8070A | 0TP/0NP | |
| DUT control interface (transportable perpetual or network license) | M8070A | 1TP/0TP | |
| 5-slot AXIe chassis with USB option | M8040A | BU2 | |
| 5-slot AXIe chassis with USB option and embedded controller M9537A | M8040A | BU1 | |
| **Calibration and productivity services** | | | **see next page** |

Figure 16. Overview of possible M8040A configurations

| Description | Product # | Option | Comment |
|---|---|---|---|
| Upgrades for M8040A High-performance BERT 64 Gbaud | M8040AU | | |
| **Pattern generator and clock module, 32/64 Gbaud, 3-slot AXIe** | **M8045A** | | |
| Upgrade to 64 Gbaud (requires remote head, M8057A) | M8045A | U64 | License |
| Upgrade to second channel, hardware and license (requires remote head, M8057A) | M8045A | UG2 | Requires return-to-factory |
| Upgrade to advanced jitter sources for receiver characterization, module-wide license | M8045A | UG3 | License |
| Upgrade to de-emphasis, module-wide license | M8045A | UG4 | License |
| Upgrade to PAM-4 encoding up to 32 Gbaud, module-wide license | M8045A | UP3 | License |
| Upgrade to extension to PAM-4 encoding up to 64 Gbaud, module-wide license | M8045A | UP6 | Only with G64/U64 |
| Remote head for M8045A pattern generator, 1 channel | M8057A | | |
| **Analyzer module, 32/64 Gbaud, 1-slot AXIe** | **M8046A** | | |
| Upgrade M8046A for data rates up to 64 Gbaud, NRZ | M8046A | U64 | Requires return-to-factory |
| Upgrade to equalization, license | M8046A | UA3 | Only with A64/U64 |
| Upgrade to PAM-4 decoding up to 32 Gbaud, license | M8046A | UP3 | License |

Figure 17. All upgrade options for M8040A are orderable under M8040AU. Most options are license options, that can be upgraded on site.

## Default accessories included with shipment

| |
|---|
| M8045A module:<br>Four 50 Ω resistors, ESD protection kit, certificate of calibration, license entitlement certificate, no signal cables, no blue sync cable |
| M8046A module:<br>One bandpass filter for clock input, ESD protection kit, certificate of calibration, license entitlement certificate, no signal cables |
| M8057A remote head:<br>includes cable connection to M8045A pattern generator module, one 50 Ω termination (2.4 mm) |
| M8040A-BU1:<br>M9505A AXIe chassis with embedded controller, USB cable, getting started guide, AXIe filler panel, power cord |
| M8040A-BU2:<br>M9505A AXIe chassis, USB cable, getting started guide, AXIe filler panel, power cord |
| M8070A:<br>CD-ROM with M8070A system software |

## Recommended accessories

| | |
|---|---|
| Short cable, 1.85 mm (m) to 1.85 mm (m), 0.15 m, 699 ps delay ± 1 ps<br>(two are recommended for each differential data output of M8057A) | M8045A-801 |
| Matched cable pair 2.4 mm (m) to 2.4 mm (m), 2 ps, length 0.85 m<br>(recommended for data input of M8046A analyzer) | M8046A-802 |
| Cable 2.92 mm (m) to 2.92 mm (m), 0.5 m<br>(recommended for clock input of M8046A analyzer) | M8046A-801 |
| M8000 sync cable (when using the system clock of M8045A for M8046A) | M8051A-801 |
| Attenuator, 6 dB, 1.85 mm | 8490G-006 |
| DC block 2.4 mm | N9398F |
| Matched directional coupler pair 50 GHz, 13 dB, 2.4 mm (recommended for external interference source RI/SI) | M8045A-802 |
| Bandpass filter 11.1 to 17.5 GHz, SMA (for M8046A clock input) | M8061A-803 |
| Microwave pick-off tees, 2.4 mm, matched pair (Qty 1 is recommend for use with N1076A/77A) | N1027A-2P2 |
| Adapter 2.4 mm (f) to 2.4 mm (f) (Qty 2 is recommended for connecting cables to pick-off tees) | 11900B |
| Adapter 3.5 mm (m) to 3.5 mm (m) (Qty 2 is recommended for connecting pick-off tees directly to N1076A/77A inputs) | 83059A |
| Rack-mount kit for AXIe 5-slot chassis M9505A | Y1226A |

## Calibration and productivity services

| | |
|---|---|
| Calibration services (3 and 5 years) | R1282 (R-50C-011-3/-5) |
| Productivity assistance | R1380-M8000 |

# Related Keysight literature

## Data sheets

| | |
|---|---|
| *J-BERT M8020A, Data Sheet* | 5991-3647EN |
| *M8030A Multi-channel BERT, Data Sheet* | 5992-1287EN |
| *M8062A 32 Gb/s Front-end, Data Sheet* | 5992-0987EN |
| *M9505A AXIe Chassis 5-slot, Data Sheet* | 5990-6584EN |
| *M8196A 92 GSa/s AWG, Data Sheet* | 5992-0971EN |
| *N1085A PAM-4 Measurement Application for 86100D DCA-X Series, Data Sheet* | 5992-1248EN |
| *N1076A/N1077A Clock recovery, Data Sheet* | 5992-1620EN |

## Application notes, white papers and posters

| | |
|---|---|
| *Characterizing and verifying compliance of 100Gb Ethernet components and systems, Application Note* | 5992-0019EN |
| *Master 400G, Poster* | 5992-2143EN |
| *Equalization: The correction and analysis of degraded signals, White Paper* | 5980-3777EN |

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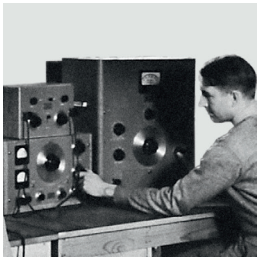
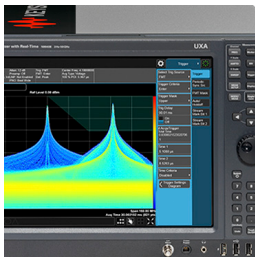


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