Agilent

N4960A Serial BERT 17 and 32 Gb/s Data Sheet

Affordable characterization and manufacturing test solution for transceivers up to 32 Gb/s

16GFC, 32GFC, 100G Ethernet, InfiniBand FDR, InfiniBand EDR, and Fast SERDES

Product Highlights

- Full data rate pattern generation and error detection
- Integrated clock source with calibrated stress capability
- Built-in selection of PRBS and common telecom/datacom test patterns
- Fully programmable user-defined patterns
- Remote heads place the signal very close to DUT

Solving the Need for Speed... Without Breaking Your Budget

Figure 1. Compact BERT solution

Verifying 100G ethernet or 16GFC transceivers requires a BERT operating beyond 13G. This often results in multiple designers needing to share the one serial BERT in the lab—delaying their characterization, along with the development schedule.

The N4960A BERT has fast transition times and real time BER count updates. In addition, low intrinsic jitter provides continuously settable clock frequencies allowing data rates from 5 to 32 Gb/s rates and from 4 to 17 Gb/s. As a result, high quality signals produce excellent fidelity in the eye for improved measurement accuracy.

The solution is compact—allowing it to be easily transported throughout the lab and manufacturing.

Compact Architecture

The N4960A-CJ0/N4960A-CJ1 serial BERT controller with jitter injection is a platform that forms the basis of the serial BERT. The controller adds the precision timing and control required for remote pattern generator and error detector heads.

Place Signal Close to DUT

The concept of remote heads, first introduced with the N4965A multi-channel BERT controller, puts the pattern generation and error detection near the device under test, eliminating long cables which degrade the signal. This is especially important beyond 17 Gb/s.

Figure 1. Place signal close to DUT

Integrated 32 Gb/s Operation

The N4951A-P32 pattern generator and N4952A-E32 error detector remote heads operate from 5 to 32 Gb/s in a single band with no gaps or missing data rates. Similarly, the N4951A-P17 pattern generator and N4952A-E17 error detector remote heads operate from 4 to 17 Gb/s in a single band with no gaps or missing data rates.

They generate and test full rate patterns directly without the need for external multiplexers and delay matching. The generator produces a selection of PRBS pattern lengths, along with a large selection of common telecom, datacom, and clock stress test patterns including K28.5, CJPAT, CJTPAT, JSPAT, JTSPAT, etc.

The signal fidelity in the eye is outstanding. Output parameters of amplitude, offset, and termination voltage are user settable.

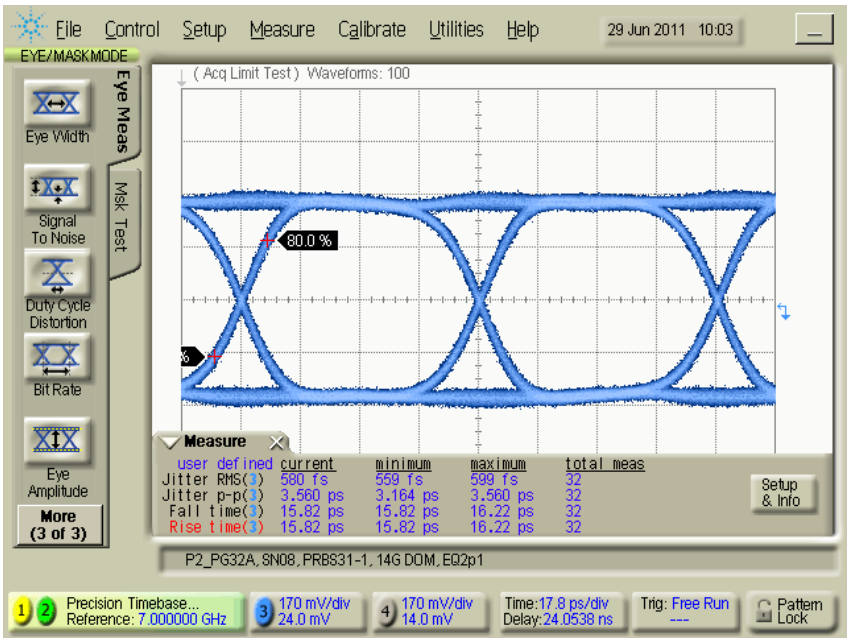


Figure 3. Typical eye at 14 Gb/s

Complete, Compact 17 Gb/s and 32 Gb/s BERT

Does your application need a full BERT? Agilent offers a surprisingly affordable total solution which includes both pattern generation and error detection capability. Tied together with our N4980A multi-instrument BERT software, this combination provides a powerful BERT solution.

Of course, the system also operates without the error detector or pattern generator, for applications which require these configurations.

For 16GFC applications operating at 14.025 Gb/s, the pattern generator and error detectors are also available in models up to 17 Gb/s. These offer even more cost effectiveness.

Choose the Complement of Stress Sources You Need

The controller is offered in two versions. The N4960A-CJ0 is the base model and is ideal for many optical serial data applications, providing a single tone of sinusoidal jitter. Settable over a wide range of frequencies and modulation depth, it facilitates jitter tolerance testing and general receiver characterization.

For applications which require a more complex “stress recipe”, the N4960A-CJ1 includes two independent sources of sinusoidal along with broadband true random jitter sources. The multiple stress generators allow you to build a low level base floor that is a mixture of random and possibly sinusoidal jitter. In addition, all three clock outputs can be modulated with spread spectrum, with a deviation settable up to 1.0 % of the clock frequency (10,000 ppm).

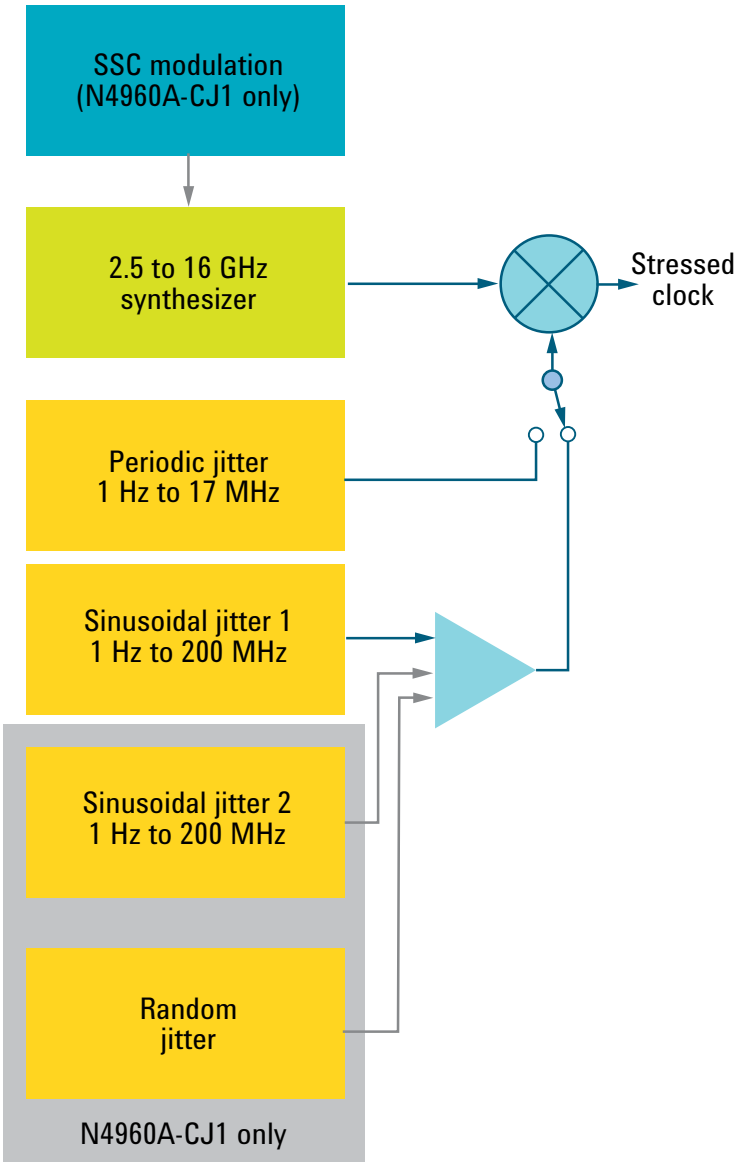


Figure 4. Stress sources

Programmable Patterns

For special pattern requirements, programmable patterns up to 8 Mb in length can be easily created with powerful editing tools built into the N4980A multi-instrument BERT software. Patterns can then be uploaded into the N4960A-CJ0/N4960A-CJ1 serial BERT controller.

The main programmable pattern editor dialog is used to create and manage pattern streams. Pattern streams are composed of one or more sub-patterns. Each sub-pattern contains a single pattern definition. Using sub-patterns allows users to break down complex patterns for easier organization.

Figure 5. Programmable pattern editor

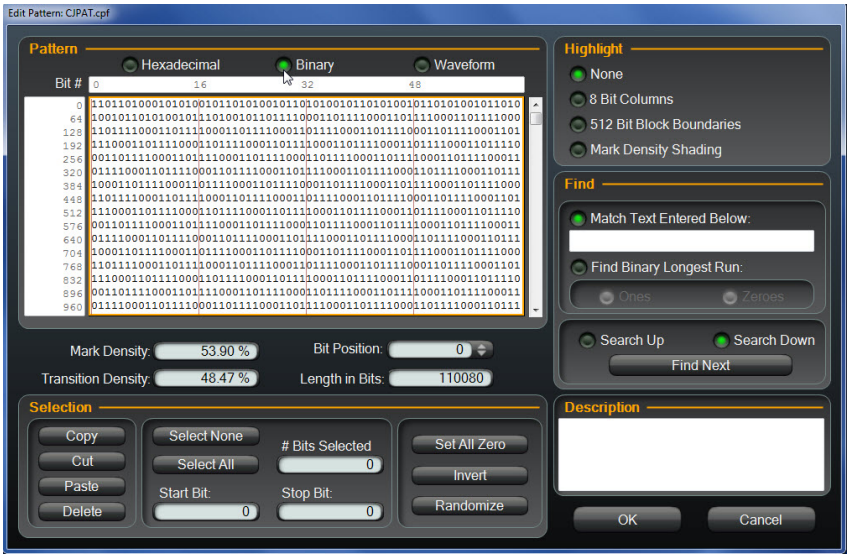


Figure 6. Sub-pattern editor

Sub-patterns can be edited at the bit level using the edit pattern dialog box. In this dialog box, users can create, view, edit, and find specific bit sequences.

Once the pattern definition is complete, it can be validated and uploaded to the N4960A-CJ0/N4960A-CJ1 serial BERT controller. It can also be saved to the PC as a *.cpf file.

Integrated Analysis Software

Support for both models of the controller is included in the N4980A multi-instrument BERT software. The base software provides an intuitive user interface and is free of charge. With the base software, you can perform single-channel BER, multi-channel BER with an unlimited number of channels, and bathtub measurements. Measurement results can be plotted or saved, as well as complete test setups. The optional jitter tolerance package adds single and multi-channel JTOL measurements with a choice of search algorithms. Testing JTOL in multi-lane devices in parallel is much faster than testing each lane individually, and more representative of the actual operating environment with live traffic present on all lanes. With the JTOL template editor, you can create templates to meet the testing criteria of the most common standards. The JTOL package requires a license to use.

Figure 7. N4980A multi-instrument BERT software

N4951A-P32/-P17 and N4952A-E32/-E17 Run at Full Rate

The N4951A-P32/N4951A-P17 pattern generator and N4952A-E32/N4952A-E17 error detector run at full rate at the input and output connectors eliminating the need for complex cabling, external multiplexers/demultiplexers, and careful calibration to align the clock phasing.

General Purpose Serial Data Clock Source

In addition to being a BERT solution, the N4960A-CJ0/N4960A-CJ1 serial BERT controller is a clock synthesizer. The N4960A-CJ0/N4960A-CJ1 can be used with other non-stressed BERTs to provide jitter capability. You can also use it for general purpose serial data characterization applications. When used as a BERT by attaching the pattern generator and error detector remote heads, the BERT settings override the settings for the clock outputs.

Three Clock Outputs

A traditional BERT setup uses a stressed (jittered) clock source for the pattern generator and a clean (non-jittered) clock for the error detector. The phase delay between these clocks must be adjustable in fine resolution of time to center the error detector sample point in the eye. The N4960A-CJ0/N4960A-CJ1 serial BERT controller has dedicated outputs for both jittered and delayed signals. In addition, a clean divided clock output is provided for applications requiring a sub rate reference, or as a trigger for sampling oscilloscopes.

Each output is configured as a differential signal but can be used single ended without the need to terminate the unused output. To address the requirements of any application, the amplitude, offset voltage, termination voltage, and coupling can be independently set on each of the three outputs.

Two Independent SJ Sources (Single Source in N4960A-CJ0 Serial BERT Controller)

For the N4960A serial BERT controller with jitter injection (SSB16000J), the stress source choices are one or two tones of high frequency sinusoidal jitter (SJ) with user settable frequency and amplitude (phase deviation). The SJ sources are summed with random jitter and any externally applied high band jitter. The frequency range of the two SJ sources is 1 Hz to 200 MHz with a modulation range of 0.001 UI to 1.0 UI (or off).

Figure 8. Clock outputs

High Deviation PJ Source

A separate modulation path is available for low frequency (high deviation) stress injection. This path is operated when all of the high frequency band (low deviation) stress sources (SJ1, SJ2, RJ, and external low deviation) are disabled. The low band path operates over lower modulation frequencies, up to 17 MHz (using internal PJ), or up to 4 MHz (external). The modulation source can be either an internally generated sinusoid (periodic jitter, or PJ), or externally supplied through the "Ext Jitter In" connector.

True Random Jitter Source (N4960A-CJ1 Serial BERT Controller)

The RJ source provides true Gaussian random jitter with a crest factor of at least 14. The unfiltered spectral content is flat from DC to the contour of the high frequency band modulator, which has –3 dB BW at approximately 320 MHz. For applications which require a specified RJ frequency contour, an external filter can be placed in the RJ modulation signal path. Both a low pass and a high pass filter can be used in series when both ends of the spectrum require filtering.

The RJ modulation range is 0 to 75 mUI-rms. However, if a filter is inserted in the RJ path, then the modulation amplitude may be attenuated from the calibrated value due to the filter attenuation.

Spread Spectrum Clock (N4960A-CJ1 Serial BERT Controller)

The main synthesizer in the N4960A-CJ1 serial BERT controller can be modulated to enable spread spectrum clocking (SSC). Spread spectrum clocking is not generally considered to be a stress, but rather a method of controlling electromagnetic interference (EMI), by spreading the peak energy of the system clock over a broad portion of the spectrum. In practice, SSC modulates the system clock in the device with a large phase deviation at a relatively low frequency, generally 30 or 33 kHz. The modulation wave shape is usually a triangle wave, to keep the power spectrum even over the modulation band. SSC is included in clock synthesizers used in BERTs to emulate a transmitter from a device which employs SSC. To assure proper tracking of the BERT or sampling scope testing a device with SSC, all three clock outputs of the N4960A-CJ1 (jittered, delayed and divided) are modulated with the same SSC signal. The SSC deviation range is 0 to 1% (1% = 10,000 ppm). The modulation envelope is a triangle waveform. The modulation frequency can be set from 1 Hz to 50 kHz. In addition, there are three settings for deviation direction: down, center, and up (relative to the clock frequency setting).

Large Library of Common Stress Patterns

The N4960A-CJ1 serial BERT controller comes with a library of stress patterns including PRBS, divided clock, JSPAT, JTSPAT, K28 series, and CJ series for optical telecom and datacom testing.

The Agilent BERT Solution

Agilent provides an affordable solution for testing jitter tolerance. The N4980A multi-instrument BERT software saves you time and money by providing a way to efficiently test jitter tolerance.

The optional JTOL measurement package performs jitter tolerance compliance and characterization. Setup is quick and easy using the jitter tolerance setup panel.

Figure 9. Jitter tolerance setup panel in N4980A

BER measurement results of each tested sinusoidal jitter point can be displayed in graphical format. A green colored dot on the graph at right indicates the point at which the receiver is passing, a red colored X indicates a synchronization issue, and the maroon colored + sign indicates the point at which the BER threshold has been exceeded.

The x-axis of the graph is SJ frequency and the y-axis is SJ amplitude. The SJ frequencies are marked by black circular markers. The compliance template is shown with a dashed line. The minimum and maximum bounds for the characterization test are shown with a solid line.

Figure 10. Jitter Tolerance Graph View

The results can also be displayed in tabular format (Figure 11) and can be saved to a file for future analysis.

Figure 11. Jitter tolerance table view

The SJ amplitude and frequency test points are defined in a template file which can be edited by simply pointing and clicking a mouse or entering the information in the numeric fields (Figure 12).

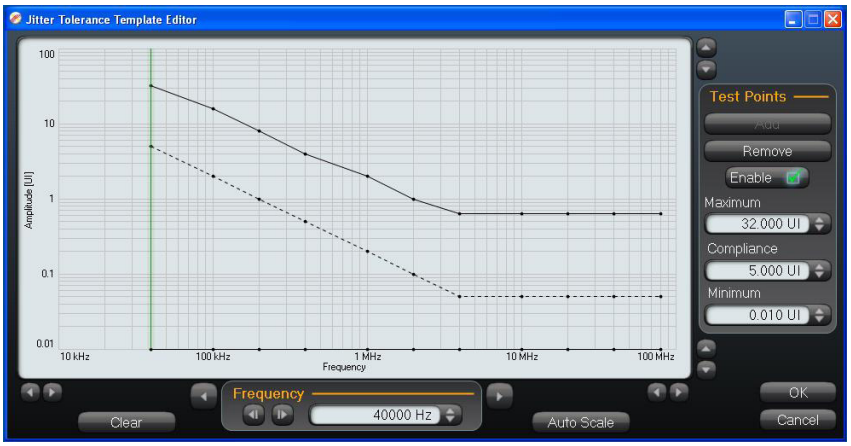


Figure 12. Template file

100G Ethernet

The 100G Ethernet is the next generation 25 Gb/s standard for evaluating chip-to-chip and chip-to-module electrical communication links within optical networks.

The example configuration below (Figure 13) requires four 25 Gb/s lanes. This is accomplished using four N4951A-P32 pattern generators to the input of the optical module. The optical module is tested in loopback mode with the receiver's electrical outputs connected to four N4952A-E32 error detectors.

This configuration supports asychronous clocking on all 4 lanes, which is required for characterizing 100GE-SR4 system components.

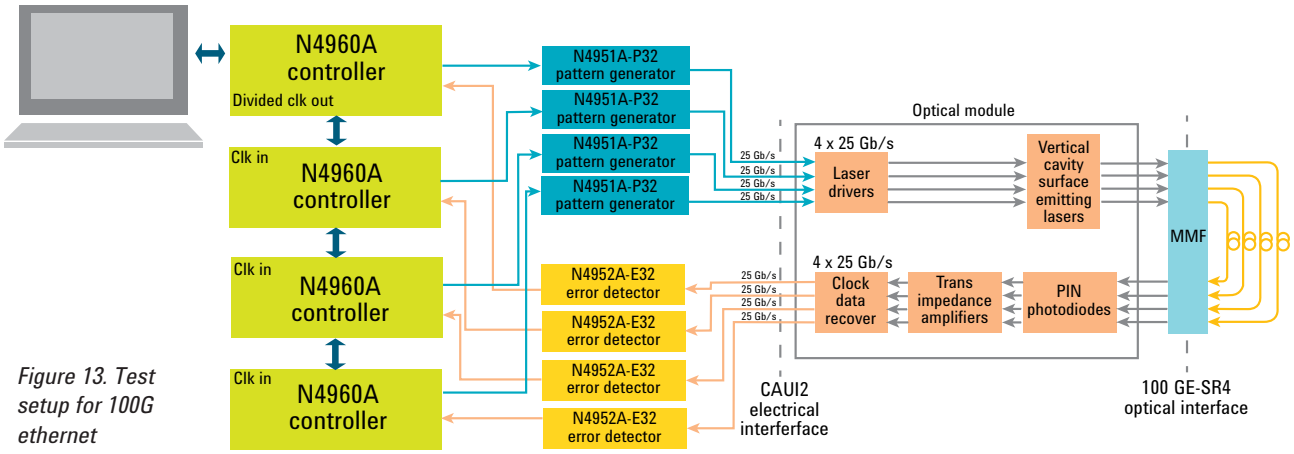


Figure 13. Test setup for 100G ethernet

Fast SerDes Design in FPGA and Other Communication ICs

SerDes circuits are often integrated into the design of FPGAs, ASICs, and other communication ICs. To ensure successful integration, SerDes circuits must be fully tested and characterized before integration.

Figure 14 shows a configuration for testing the received data through a loopback in a SerDes. The BER and jitter tolerance can be measured at all rates using the N4951A-P32/ N4952A-E32 (32 Gb/s) on the transmit side of a SerDes. Likewise, the BER and jitter tolerance can be measured at all rates using the N4951A-P17/N4952A-E17 (17 Gb/s) on the transmit side of a SerDes as well.

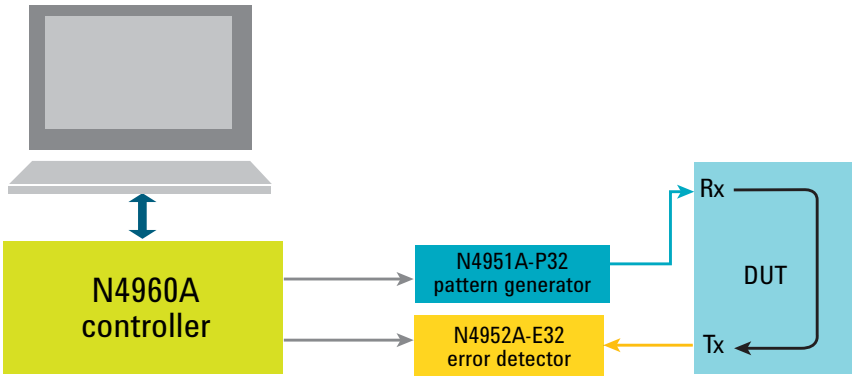


Figure 14. Test setup for communication ICs

The pattern editor in the N4980A multi-instrument BERT software enables the design of stress patterns and pattern streams for the specific application. In addition, the software simplifies the task of setting up and running BER and jitter tolerance tests.

16GFC

Testing 16GFC devices requires equipment capable of 14.025 Gb/s. Used in the storage, computing, and communications industries, 16GFC devices must be accurately characterized to strict tolerances.

A basic configuration using the 17 Gb/s BERT system is shown above. N4951A-P17 and N4952A-E17 (PG17 and ED17) can be loaded with common stress patterns for 16GFC. You can also custom design your own patterns up to 8 Mb in length and upload them into the N4951A-P17 and N4952A-E17 (PG17 and ED17).

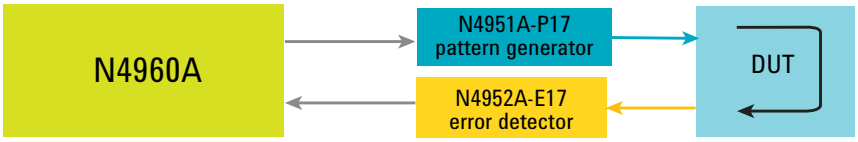


Figure 15. Test setup for 16GFC

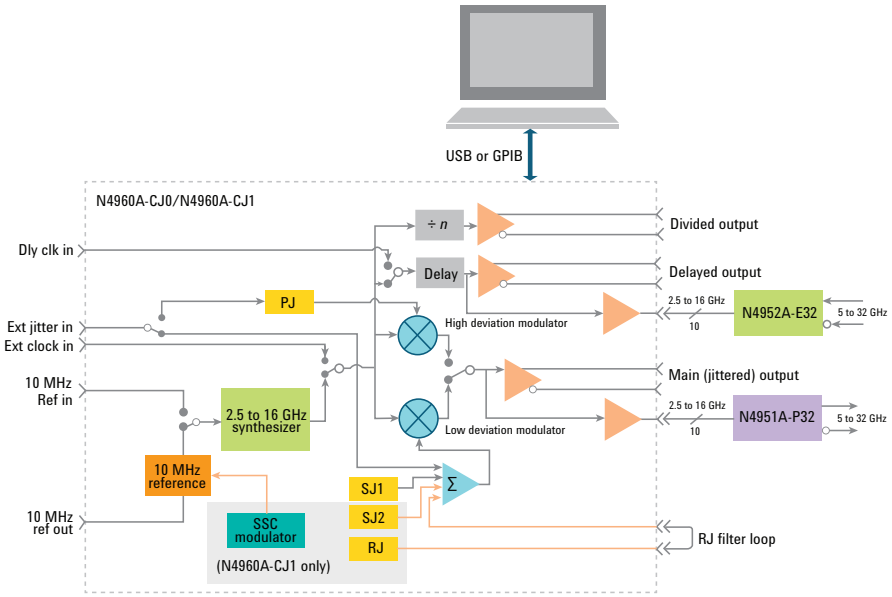


Figure 16. Block diagram (32 Gb/s system)

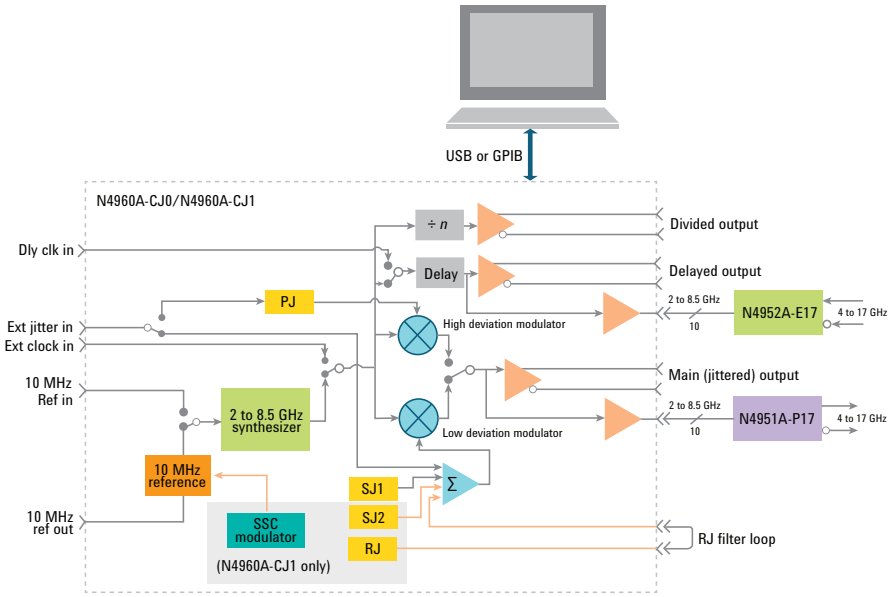


Figure 17. Block diagram (17 Gb/s system)

N4960A-CJ0/N4960A-CJ1 Synthesizer Specifications

Configuration	Frequency synthesizer with three outputs: jitter (stressed), delay, and divided (both non-stressed). Clock generator jitter and delay outputs are shared with pattern generator and error detector. Changing front panel output parameters while pattern generator and error detector are operating will effect BERT operation. N4951A-P32/-P17 and N4952A-E32/-E17 use double data rate architecture. The BERT data rate is double the frequency of the front panel clock outputs, and the pattern generator stress outputs will be doubled in amplitude
Frequency	2 to 16 GHz 2 to 8.5 GHz (restricted when N4951A-P17 or N4952A-E17 is attached)
Frequency resolution	1 kHz (front panel)
Outputs	Jitter (stressed), delay, and divided (non-stressed)
Output configuration (all outputs)	Differential, with amplitude, offset and termination voltage adjustment (can be used single ended without terminating unused outputs)
Amplitude range	300 mV to 1.7 V (p-p), single ended
Offset range	–2.4 to +2.4 V (limited by termination voltage, see Figure 18) On divided clock output, this is only valid when the divide ratio is a power of 2.
Termination voltage range	–2.4 to +2.4 V (limited by offset voltage, see Figure 18)
Rise time (20% to 80%)	< 20 ps
Intrinsic jitter	< 800 fs rms, integrated from 1 kHz to 100 MHz, for clock frequencies ≥ 1 GHz < 1.2 ps rms for clock frequencies < 1 GHz
Duty cycle	
Jitter and delay outputs	50% ±5%
Divided output	50% ±5% at divide ratios which are a power of 2 Duty cycle may not be 50% at divide ratios which are not a power of 2 50% ±10% when divide ratio is set to 1 for amplitudes ≥ 500 mV
Frequency stability	0.1 ppm
Frequency accuracy	±20 ppm
Reference frequency	10.0 MHz, single ended output and input on rear panel
External clock	Single ended input can be substituted for internal synthesizer
External delayed clock input	Single ended input can be substituted for internal synthesizer
Spread spectrum clock (N4960A-CJ1 serial BERT controller only)	Phase deviation appears on all outputs
Deviation range	0 to 1.0% (10,000 ppm)
Modulation frequency range	1 Hz to 50 kHz
Modulation wave shape	Triangle
Deviation direction	Down spread, center spread, or up spread
Divided clock divide ratio	÷ 1, 2, 3,..., 99,999,999, with no missing integers (waveshape of divided clock slower than ≈1 MHz will be differentiated)
Delayed clock delay range	0 to ±1,000 UI
Delayed clock delay resolution	10 mUI
Connector type	
All signals except 10 MHz ref in/out	SMA
10 MHz ref in, out	BNC

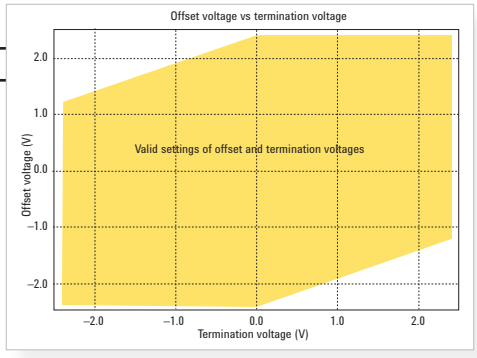


Figure 18. Maximum offset and termination voltage ranges

N4960A-CJ0/N4960A-CJ1 Synthesizer Stress Specifications

Configuration	Calibrated stress is added to jitter clock output and the pattern generator clock through one of two modulators: a high deviation, low frequency path, or a low deviation, high frequency path. The amplitude of any stress appearing on the front panel jitter clock output will be ½ of the value appearing in the N4951A-P32/-P17 output. Changing stress amplitudes on the front panel jitter clock output will also change the level appearing on the pattern generator output.
Sources	
N4960A-CJ0	Single tone sinusoidal jitter, low and high deviation, plus external input
N4960A-CJ1	Two internal sinusoidal jitter, true random jitter, plus external input
SJ frequency range	1 Hz to 200 MHz
SJ modulation range N4951A-P32	Range of SJ1 and SJ2. The maximum combined peak jitter of SJ1 + SJ2 + RJ (p-p) + external jitter are applied to the high frequency band modulator (see Figures 19 and 20).
Front panel output frequency > 2.5 GHz to 3 GHz (N4951A-P32 not connected)	0.01 to 1.0 UI pk for modulation frequency 1 Hz to 100 MHz, 0.01 to 0.5 UI pk for modulation frequency > 100 MHz to 200 MHz
Front panel output frequency > 2.5 GHz to 3 GHz (N4951A-P32 not connected)	0.01 to 0.5 UI pk for modulation frequency 1 Hz to 200 MHz
Front panel output frequency > 3 GHz to 16 GHz (N4951A-P32 not connected)	0.01 to 1.0 UI pk for modulation frequency 1 Hz to 100 MHz, 0.01 to 0.7 UI pk for modulation frequency > 100 MHz to 200 MHz
Front panel output frequency > 3 GHz to 16 GHz (N4951A-P32 not connected)	0.01 to 0.5 UI pk for modulation frequency 1 Hz to 200 MHz
SJ modulation range, N4951A-P17	Range of SJ1 and SJ2; the maximum combined peak jitter of SJ1 + SJ2 + RJ (p-p) + external jitter are applied to the high frequency band modulator (see Figures 21 and 22).
Front panel output frequency > 2 GHz to 3 GHz (N4951A-P17 not connected)	0.01 to 1.0 UI pk for modulation frequency 1 Hz to 100 MHz, 0.01 to 0.5 UI pk for modulation frequency > 100 MHz to 200 MHz
Front panel output frequency > 2 GHz to 3 GHz (N4951A-P17 not connected)	0.01 to 0.5 UI pk for modulation frequency 1 Hz to 200 MHz
Front panel output frequency > 3 GHz to 8.5 GHz (N4951A-P17 not connected)	0.01 to 1.0 UI pk for modulation frequency 1 Hz to 100 MHz, 0.01 to 0.7 UI pk for modulation frequency > 100 MHz to 200 MHz
Front panel output frequency > 3 GHz to 8.5 GHz (N4951A-P17 not connected)	0.01 to 0.5 UI pk for modulation frequency 1 Hz to 200 MHz
RJ modulation frequency contour	Flat from DC to modulator band pass: –3 dB @ 320 MHz, single pole roll off to 500 MHz. Loop through allows user to customize contour by inserting HPF or LPF in loop on rear panel. Nominal impedance is 50 Ω. Filter insertion loss will lower RJ modulation depth below calibrated value
RJ modulation range (N4951A-P32/-P17 not connected)	0 to 75 mUI rms, can be set up to 150 mUI rms, to allow for insertion loss in external filters, but is uncalibrated for settings > 75 mUI. Peak sum of all SJ, RJ and External input applied to high frequency modulation input is limited. Refer to SJ modulation range specification or Figures 19 or 21.
RJ modulation range (N4951A-P32/-P17 connected)	0 to 25 mUI rms maximum
RJ crest factor	14 minimum (p-p to rms ratio)

External high frequency band input	
Configuration	Wide band low deviation external modulation input. External input is summed with SJ1, SJ2, and RJ. High frequency band stress is not available when either low frequency PJ or external is selected.
Modulation frequency range	DC to at least 350 MHz, determined by high frequency modulator. –3 dB BW » 320 MHz
Modulation Range	peak sum of all SJ, RJ and external input applied to high frequency modulation input is limited. Refer to SJ modulation range specification or Figures 19 through 22.
Low frequency (high deviation) modulation configuration	Periodic jitter (PJ) or external input. SJ, RJ and high frequency external modulation sources are not available when either low frequency source is enabled.
Low frequency modulation frequency range	
PJ	1 Hz to 17 MHz
External	1 Hz to 4 MHz
Low frequency PJ modulation range	
Front panel main clock output	0.001 to 100 UI for frequency ≤ 62.5 kHz
(N4951A-P32/-P17 not connected)	0.001 to (6.25E6/ PJ frequency) for frequency > 62.5 kHz to 17 MHz (see Figure 19)
Front panel main clock output	0.001 to 50 UI for frequency ≤ 62.5 kHz
(N4951A-P32/-P17 connected)	0.001 to (3.125E6/ PJ frequency) for frequency > 62.5 kHz to 17 MHz (see Figure 20)
Low frequency external modulation range	
Front panel main clock output	0.001 to 50 UI for frequency ≤ 68.4 kHz
(N4951A-P32/-P17 not connected)	0.001 to (3.42E6/modulation frequency) for frequency > 8.4 kHz to 4 MHz (see Figure 19 or 21)
Front panel main clock output	0.001 to 25 UI for frequency ≤68.4 kHz
(N4951A-P32/-P17 connected)	0.001 to (1.71E6/modulation frequency) for frequency > 68.4 kHz to 4 MHz (see Figure 20 or 22)

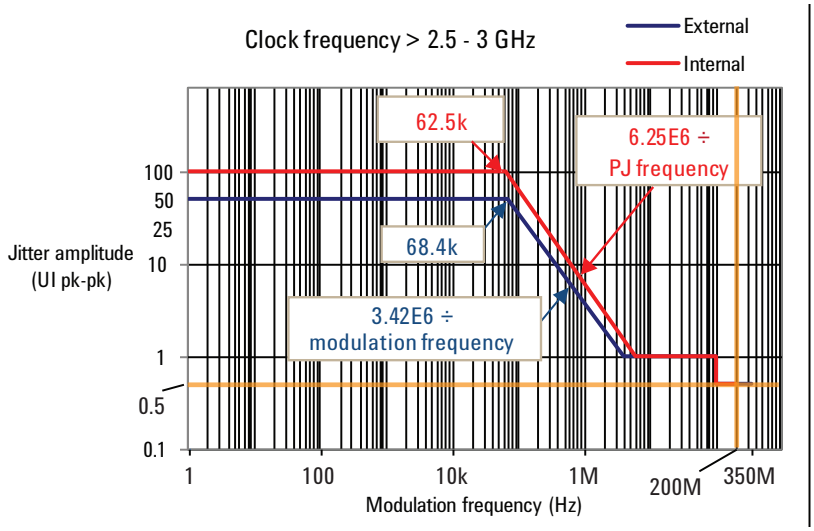


Figure 19a. Clock frequency > 2.5 to 3 GHz; modulation amplitude range graphs without N4951A-P32 connected

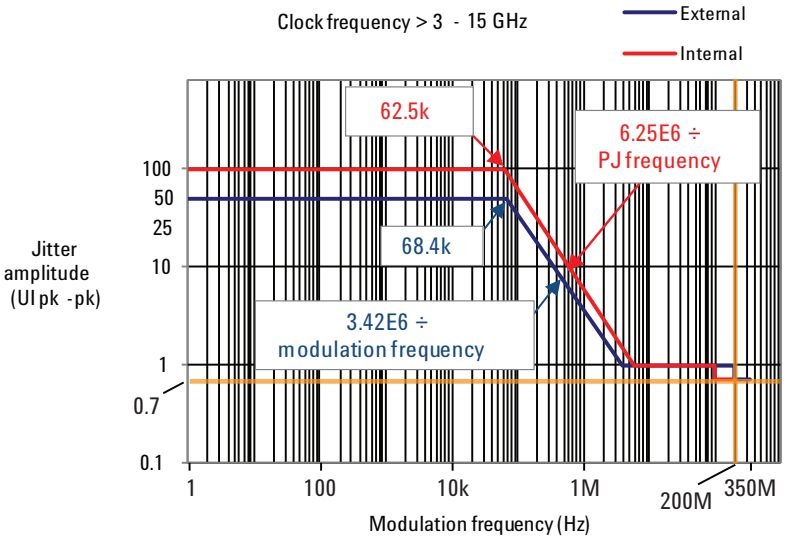


Figure 19b. Clock frequency > 3 to 15 GHz; modulation amplitude range graphs without N4951A-P32 connected

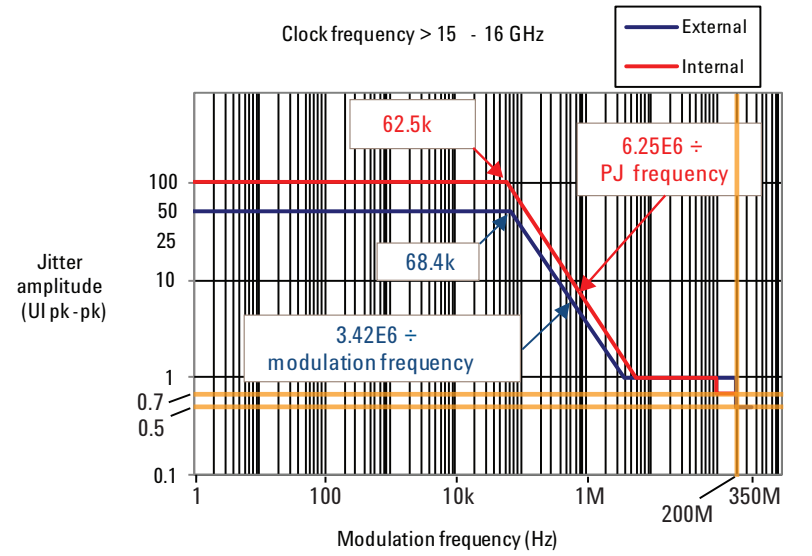


Figure 19c. Clock frequency > 15 to 16 GHz; modulation amplitude range graphs without N4951A-P32 connected

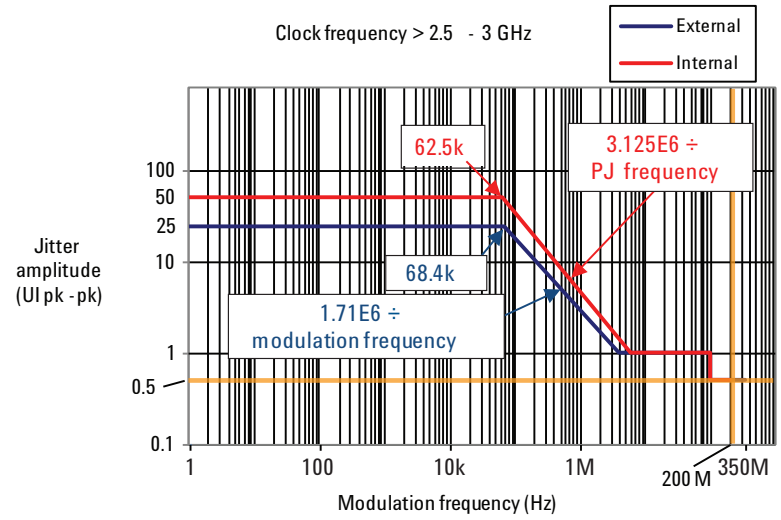
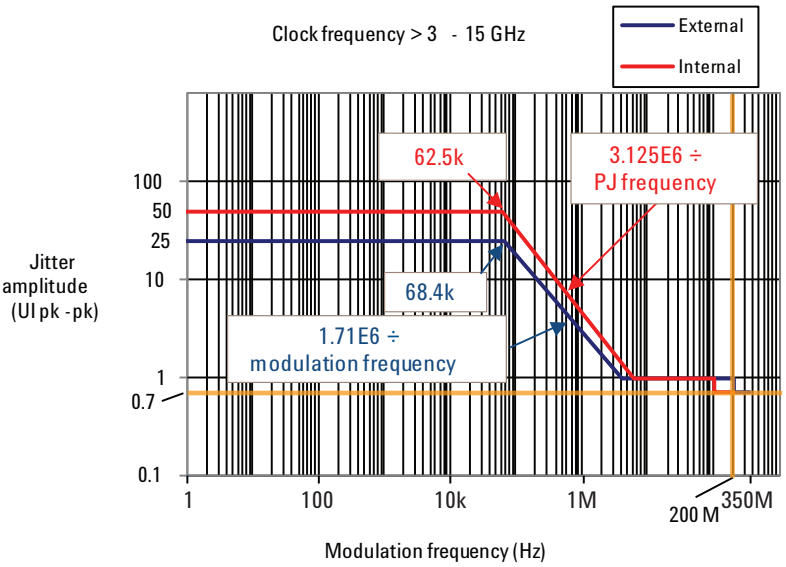
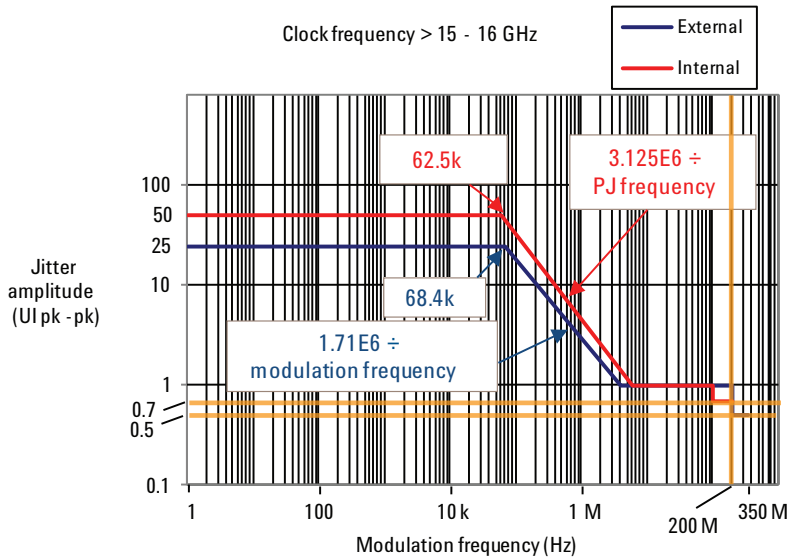


Figure 20a. Clock frequency > 2.5 to 3 GHz; modulation amplitude range graphs with N4951A-P32 connected



Figures 20b. Clock frequency > 3 to 15 GHz; modulation amplitude range graphs with N4951A-P32 connected



Figures 20c. Clock frequency > 15 to 16 GHz; modulation amplitude range graphs with N4951A-P32 connected

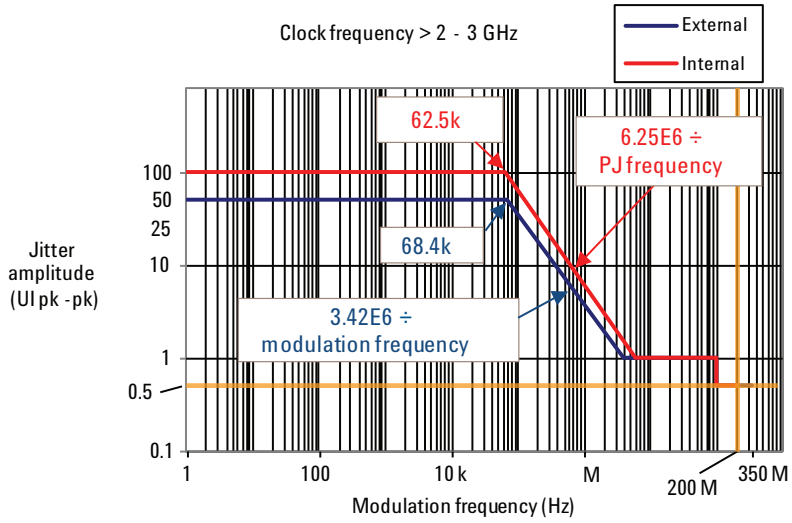
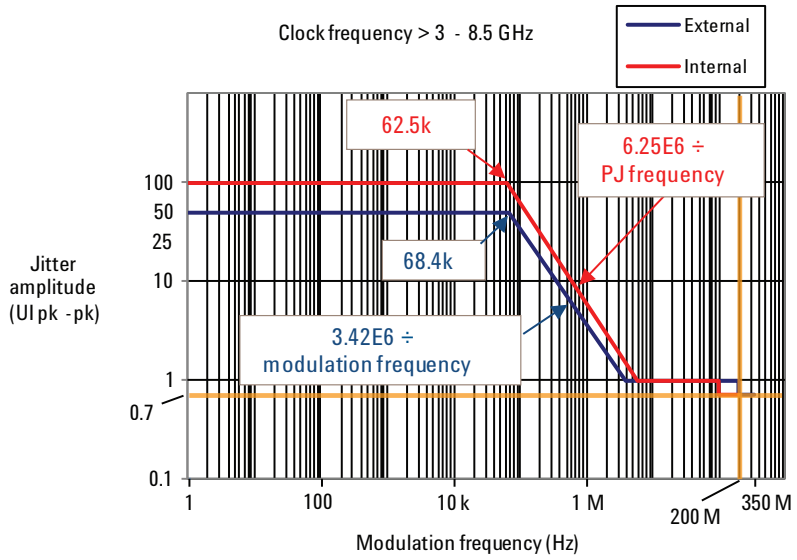


Figure 21a. Clock frequency > 2 to 3 GHz; modulation range without N4951A-P17 connected



Figures 21b. Clock frequency > 3 to 8.5 GHz; modulation amplitude range graphs without N4951A-P17 connected

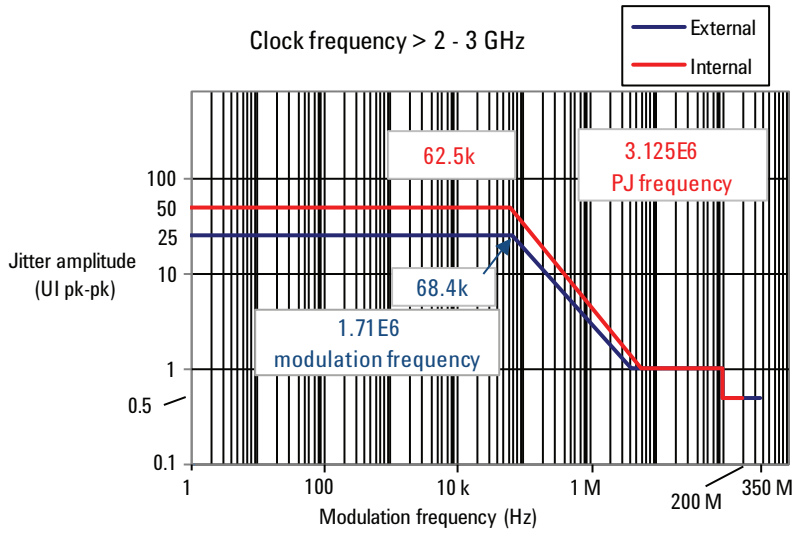
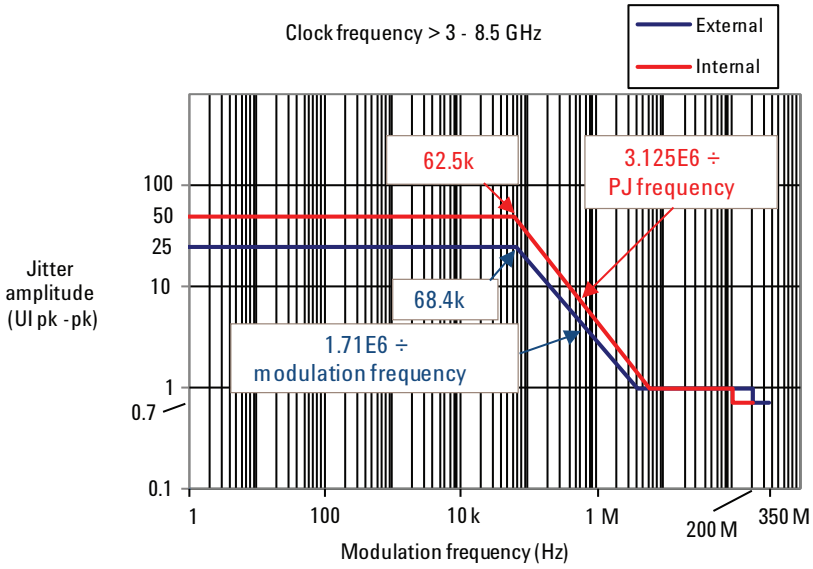


Figure 22a. Clock frequency > 2 to 3 GHz; modulation range with N4951A-P17 connected



Figures 22a and b. Clock frequency > 3 to 8.5 GHz; modulation amplitude range graphs with N4951A-P17 connected

N4951A-P32/-P17 Pattern Generator Remote Head Specifications

Configuration	Remote mountable head operates with N4960-CJ0 / N4960A-CJ1.
Data rate range (N4951A-P32)	5 to 32.0 Gb/s
Data rate range (N4951A-P17)	4 to 17.0 Gb/s
Data rate resolution	2 kb/s
Pattern selection	
PRBS (hardware generated)	$2^n - 1$, n = 7, 9, 10, 11, 15, 23, 29, 31, 33, 35, 39, 41, 45, 47, 49, 51
Telecom/datacom	K28.3, K28.5, K28.7, CJPAT, CJTPAT, CRPAT, JSPAT, JTSPAT
Clock	÷ 2, ÷ 4, ÷ 8, ..., ÷ 64, ÷ 2 = 0101, ÷ 4 = 0011, ..., ÷ 64 = 32 0's followed by 32 1's
User	1 bit to 8 Mb
Pattern invert	Available for all patterns
Error injection	Single or uniform rate
Error injection rates	10^{-n}, n = 3, 4, 5, 6, 7, 8, 9
Output configuration	Differential. May be operated single end without unused output terminated into 50 Ω. AC Coupled with internal bias tee
Output connectors	Type 'K' (2.92 mm)
Output amplitude	100 mV (p-p) to 1.0 V (p-p), single ended
Offset voltage range	–2 V to +2 V. Offset range limited by termination voltage
Termination voltage range	–2 V to +2 V. Termination voltage limited by offset voltage
Rise time (20% to 80%)	15 ps typical
SJ modulation range	Range of SJ1 and SJ2. The maximum combined peak jitter of SJ1 + SJ2 +RJ (p-p) + external jitter are applied to the high frequency band modulator (see Figures 19 and 20).
RJ modulation range	50 mUI rms maximum
Low frequency PJ modulation range	See Figures 19 through 22
Low frequency external modulation range	See Figures 19 through 22
High frequency external modulation range	Range of SJ1 and SJ2. The maximum combined peak jitter of SJ1 + SJ2 +RJ (peak) + external jitter are applied to the high frequency band modulator. 0.8 UI (p-p) up to 200 MHz 0.6 UI (p-p) from 200 MHz to 300 MHz
Indicators	Ch ID – connected to SSB16000 channel Atten – error condition occurred and logged in error log On – data output on

N4952A-E32/-E17 Error Detector Remote Head Specifications

Configuration	Remote mountable head operates with N4960A-CJ0/N4960A-CJ1.
Data rate range (N4952A-E32)	5 to 32.0 Gb/s
Data rate range (N4952A-E17)	4 to 17.0 Gb/s
Data rate resolution	2 kb/s
Pattern selection	
PRBS (hardware generated)	2n – 1, n = 7, 9, 10, 11, 15, 23, 29, 31, 33, 35, 39, 41, 45, 47, 49, 51
Telecom/datacom	K28.3, K28.5, K28.7, CJPAT, CJTPAT, CRPAT, JSPAT, JTSPAT
Clock	÷ 2, ÷ 4, ÷ 8, ..., ÷ 64. ÷ 2 = 0101, ÷ 4 = 0011 ,..., ÷ 64 = 32 0's followed by 32 1's
User	1 bit to 8 Mb
Input configuration	Differential. May be single end with unused output terminated into 50 Ω (termination included), AC coupled with internal bias tee
Input connectors	Type 'K' (2.92 mm)
Input range	100 mV to 1 V (p-p) single ended
Termination voltage	–2 V to +2 V
Indicators	Ch ID – connected to SSB16000 channel Run – BER measurement running Errors – bit errors occurring Data loss – no data detected Sync loss – not synchronized to the incoming data stream Atten – error condition occurred and recorded into error log

General Specifications

Remote Control Interface	USB2.0 and IEEE-488 (GPIB)
Power Requirements	
Voltage	100 to 240 VAC, auto-ranging
Frequency	50 to 60 Hz
Power Consumption	145 W maximum
Temperature, Operating	+10° to +40° C
Temperature, Non-Operating	–40° to +70° C
Dimensions (Height, Width, and Depth)	
N4960A-CJ0 / N4960A-CJ1	100 mm (3.9 in) x 214 mm (8.4 in) x 425 mm (16.7 in)
N4951A-P32/N4952A-E32	50 mm (1.9 in) x 109 mm (4.3 in) x 222 mm (8.7 in)
N4951A-P17/N4952A-E17	50 mm (1.9 in) x 109 mm (4.3 in) x 222 mm (8.7 in)
PG/ED Cable Length	1.0 m (39.7 in)
Mass	
N4960A-CJ0 / N4960A-CJ1	3.2 kg (7.0 lbs)
N4951A-P32/N4952A-E32 (with cable)	0.86 kg (30.3 oz)
N4951A-P17/N4952A-E17 (with cable)	0.86 kg (30.3 oz)

Regulatory Standards

EMC	
Complies with European EMC Directive 2004/108/EC	• IEC/EN 61326-1 • CISPR Pub 11 Group 1, class A • AS/NZS CISPR 11 • ICES/NMB-001
	This ISM device complies with Canadian ICES-001. Cet appareil ISM est conforme a la norme NMB-001 du Canada.
Safety	
Complies with European Low Voltage Directive 2006/95/EC	• IEC/EN 61010-1, 2nd Edition • Canada: CSA C22.2 No. 61010-1 • USA: UL std no. 61010-1, 2nd Edition
German Acoustic statement	
Acoustic noise emission	Geraeuschemission
LpA < 70 dB	LpA < 70 dB
Operator position	Am Arbeitsplatz
Normal position	Normaler Betrieb
Per ISO 7779	Nach DIN 45635 t.19

Ordering Information

All accessories required for operation are shipped with the system.

Serial BERT 32 Gb/s

Model number	Description
N4960A-CJ0 serial BERT controller	Serial BERT controller
N4960A-CJ1 serial BERT controller with jitter injection	Serial BERT controller with multi-tone jitter
N4951A-P32	5 to 32 Gb/s pattern generator remote head
N4952A-E32	5 to 32 Gb/s error detector remote head

Serial BERT 17 Gb/s

Model number	Description
N4960A-CJ0 serial BERT controller	Serial BERT controller
N4960A-CJ1 serial BERT controller with jitter injection	Serial BERT controller with multi-tone jitter
N4951A-P17	4 to 17 Gb/s pattern generator remote head
N4952A- E17	4 to 17 Gb/s error detector remote head

Model number	Description
N4980A	Multi-instrument BERT software
N4980A-JTS	Jitter tolerance software package

Warranty and Calibration Service

For warranty and calibration service information, contact your local authorized Agilent distributor or Agilent sales department.

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