10GHz Timing and 4+ Gb/s State probe for DDR4 DIMMs

Exclusively for Keysight U4164 Logic Analyzers

➢ **Industry only DDR4 10 GHz Timing and 4+ Gb/s Read and Write State Analysis from a single probe point**

➢ **It's like a 102 channel 10GHz scope !**

➢ **Designed exclusively for use with 3 Keysight U4164 logic analyzer modules in ¼ channel Timing and Quad Sample State modes**

➢ **Easiest way ever to get complete bus insight on boot issues**

➢ **Interposer design does not consume a slot**

➢ **Single point probing provides biggest eyes possible**

NEW

FS2520 DDR4 DIMM Quarter Channel Timing and Quad Sample State Interposer

Key Features

➢ Quick and easy connection between the 288 pin DDR4 DIMM memory bus connector and 3 U4164 Keysight logic analyzer modules

➢ All signals are just passively single probed, which allows for the least intrusive DDR4 interposer design done to date

➢ Complete and accurate 4+ Gb/s State mode and 10GHz Timing mode on all DDR4 bus signals

➢ Does not require U4201A probe cables

➢ Registered, Unbuffered, and Load Reduced (LR) DIMMs are all supported

➢ Captures **Writes and Reads at the same time**

➢ Quick and easy setup using Keysight EyeScan with 5 ps resolution

Straightforward, Reliable DDR4 10GHz Timing and >4Gb/s State Analysis

The FuturePlus® FS2520 DDR4 DIMM Timing and State Interposer provides a mechanical, electrical and software interface between an Keysight U4164 logic analyzer and the DDR4 connector. The FS2520 is used to design and debug computer motherboards and DIMMs incorporating DDR4 technology.

Helping you Design Tomorrow's Computers, Today
FuturePlus Systems is the technology leader in protocol analysis tools for the computer design industry. Our Interposers and software help you monitor and verify complex activities on your advanced technology computer bus design. FuturePlus systems offerings include bus-analysis solutions for most popular computer buses. Visit www.futureplus.com for more information.
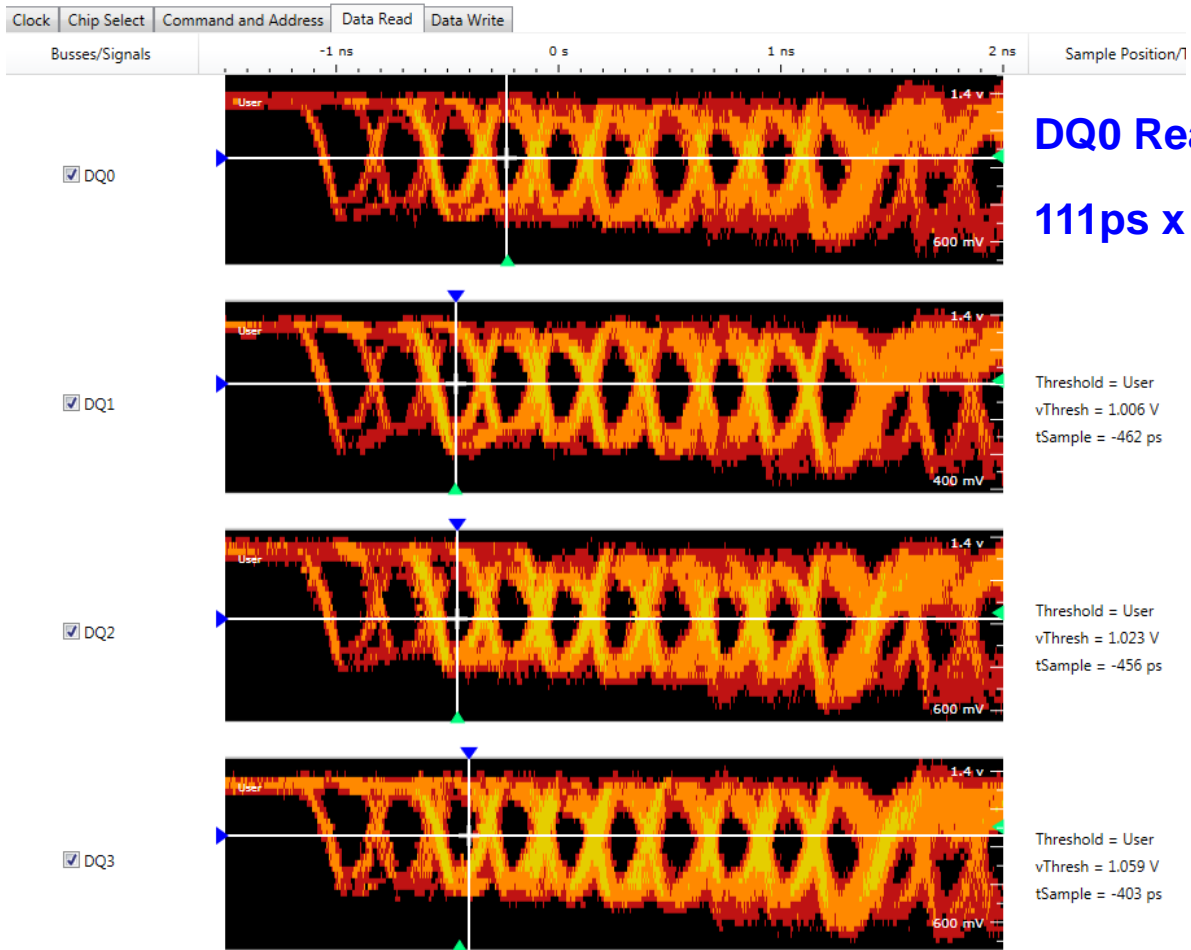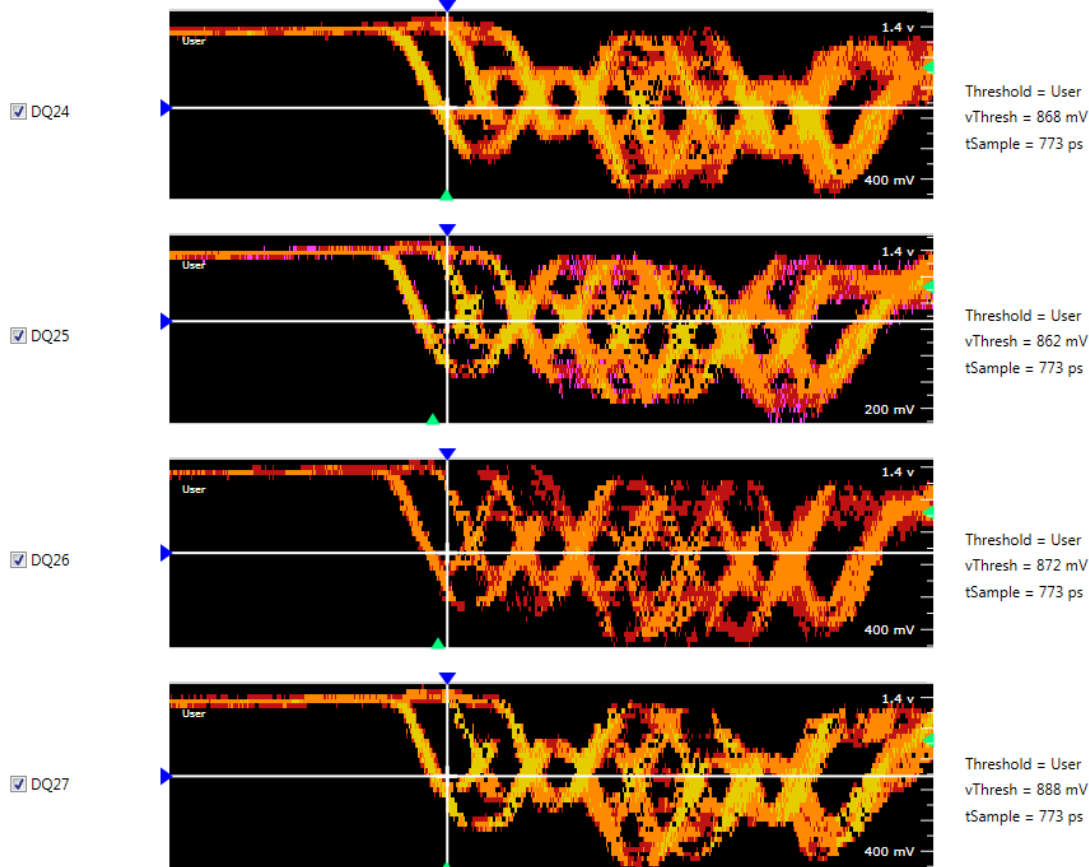
Oscilloscope quality insight on all Data signals at the same time!

4133 MT/s DDR4 READ Eyes from Burstscan Display on the FS2520

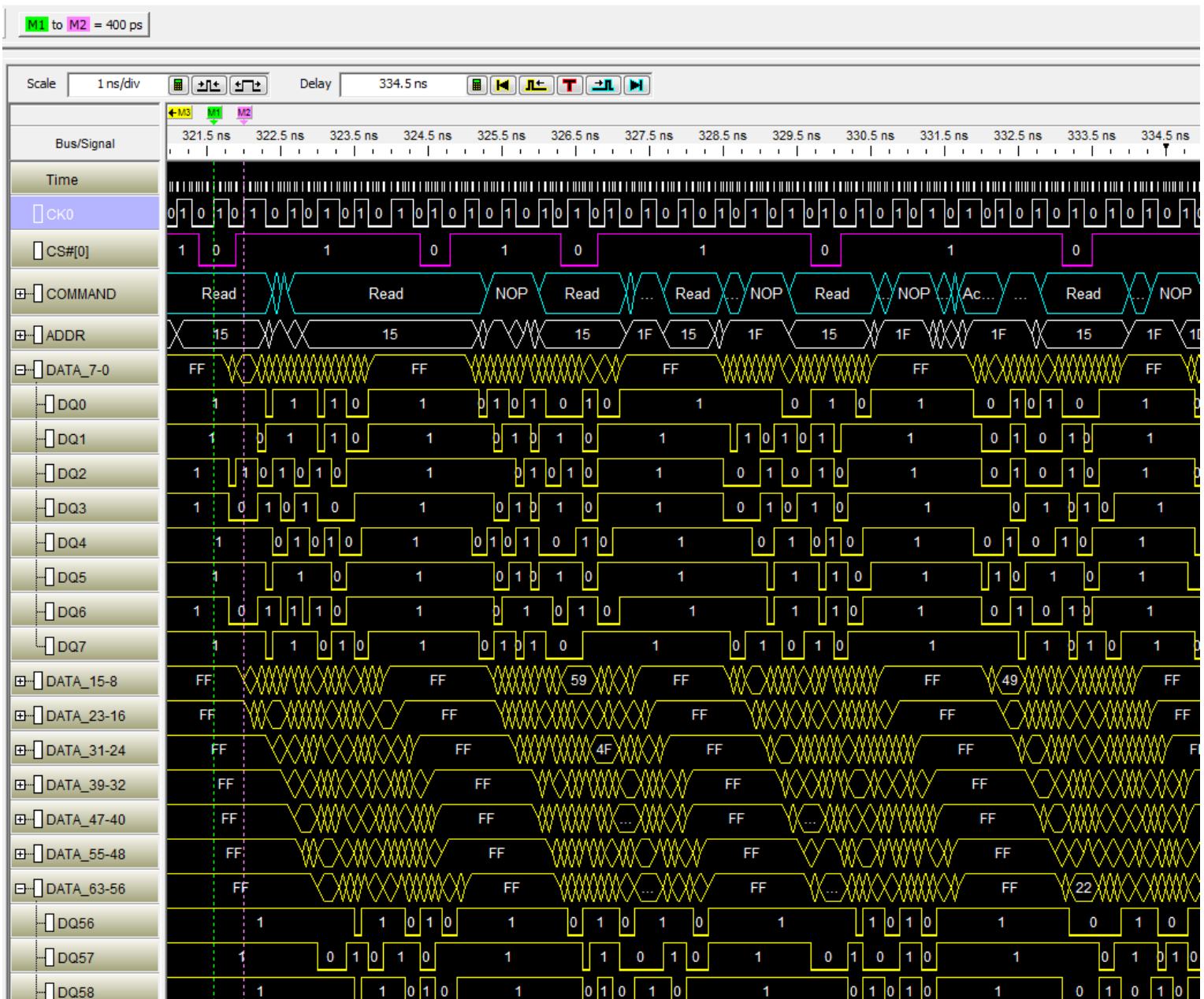| Clock | Chip Select | Command and Address | Data Read | Data Write |

DQ0 Read eye

111ps x 250mV

Threshold = User
vThresh = 1.006 V
tSample = -462 ps

Threshold = User
vThresh = 1.023 V
tSample = -456 ps

Threshold = User
vThresh = 1.059 V
tSample = -403 ps

4133 MT/s DDR4 WRITE Eyes from Burstscan Display on the FS2520

Threshold = User
vThresh = 868 mV
tSample = 773 ps

Threshold = User
vThresh = 862 mV
tSample = 773 ps

Threshold = User
vThresh = 872 mV
tSample = 773 ps

Threshold = User
vThresh = 888 mV
tSample = 773 ps
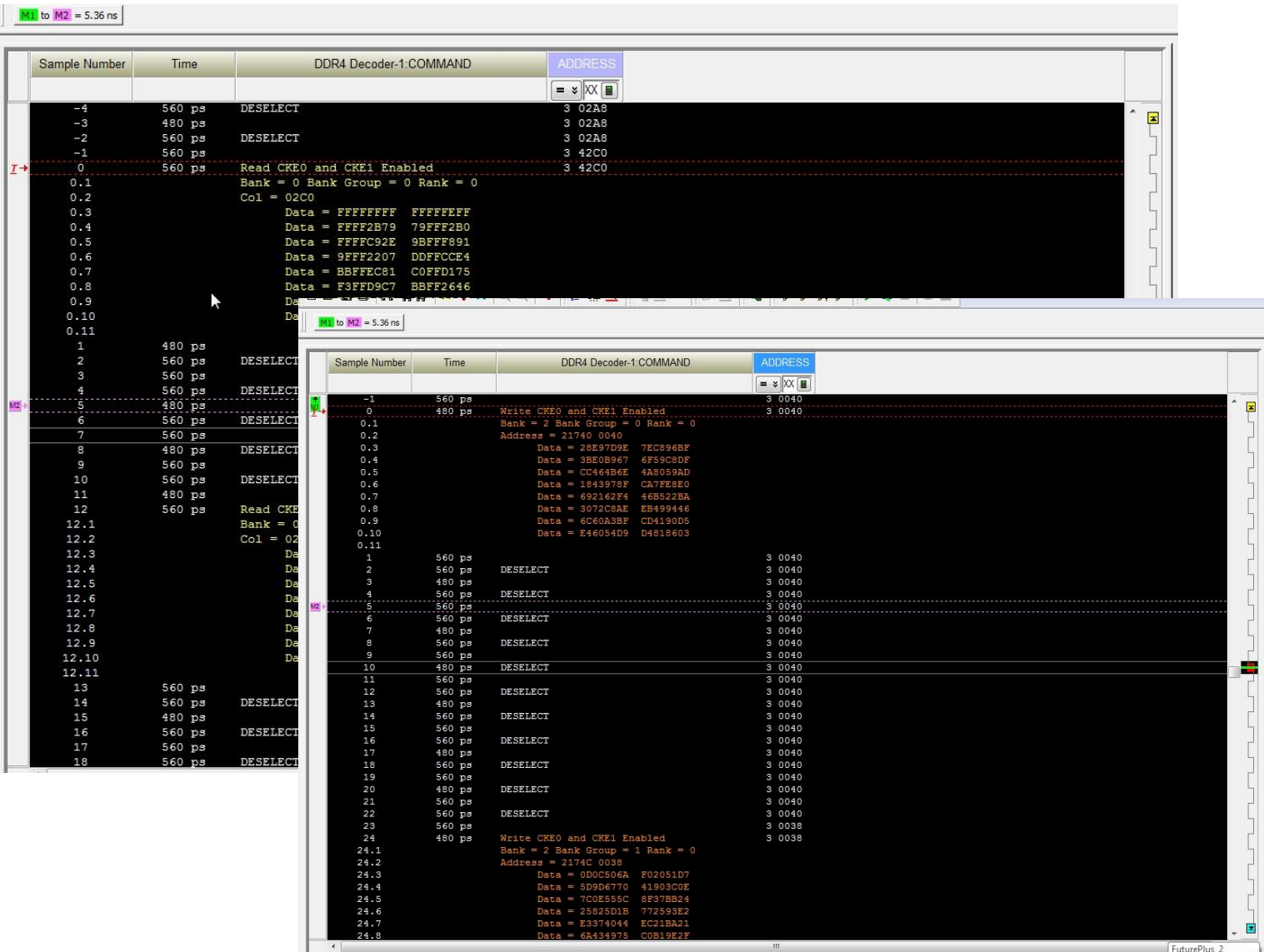
10GHz deep Timing Analysis

102 channels of Oscilloscope quality 10GHz asynchronous visibility with deep Quarter Channel Timing mode analysis.

This is a breakthrough technical capability of the U4164A and provides a unique tool for debugging issues where the bus clock may not be stable, like boot problems.

Accurate State Analysis

The FS2520 DDR4 DIMM memory bus interposer brings bus signals directly to 3 U4164A Keysight logic analyzer modules via controlled impedance cables for an easy timing and protocol analysis connection while maintaining signal fidelity.

Simultaneous READ and WRITE State Capture at 4000MT/s
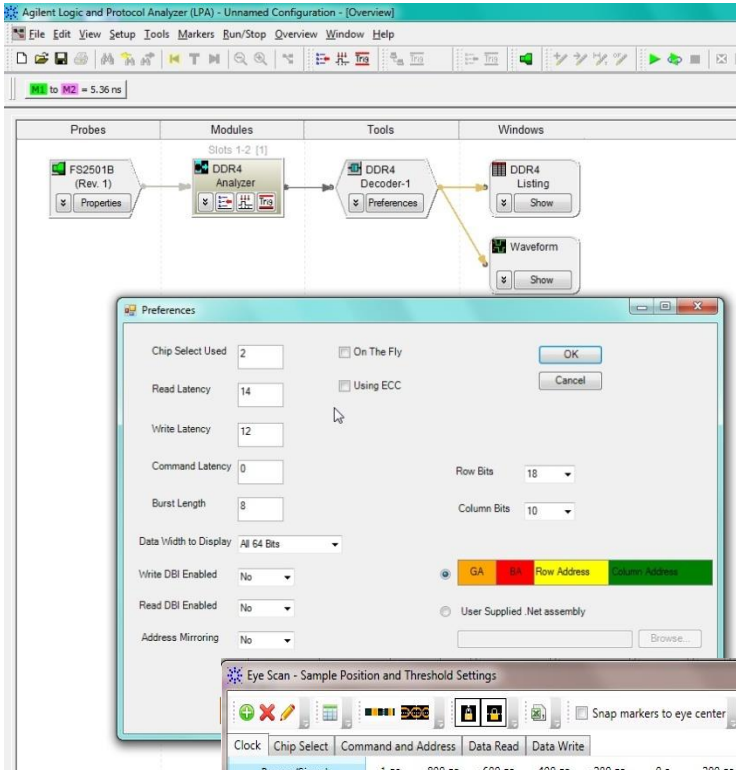

The FS2520 Keysight provided protocol-decode software translates acquired signals into easily understood bus transactions, at the full bus speed. The U4164 Keysight logic analyzer provides extensive triggering and store qualification features.

The DDR protocol decode software executes in the logic analyzer and takes user input on system attributes such as Burst Length, CAS and Additive Latency, as well as Chip Selects to decode the key DDR bus signals and present a display that lists the transaction type, address, data and command conditions. The software also supports user-defined symbols that can be easily added to the state listing display. User-selectable post-processing filters allow the acquired data to display different types of transactions in different colors.

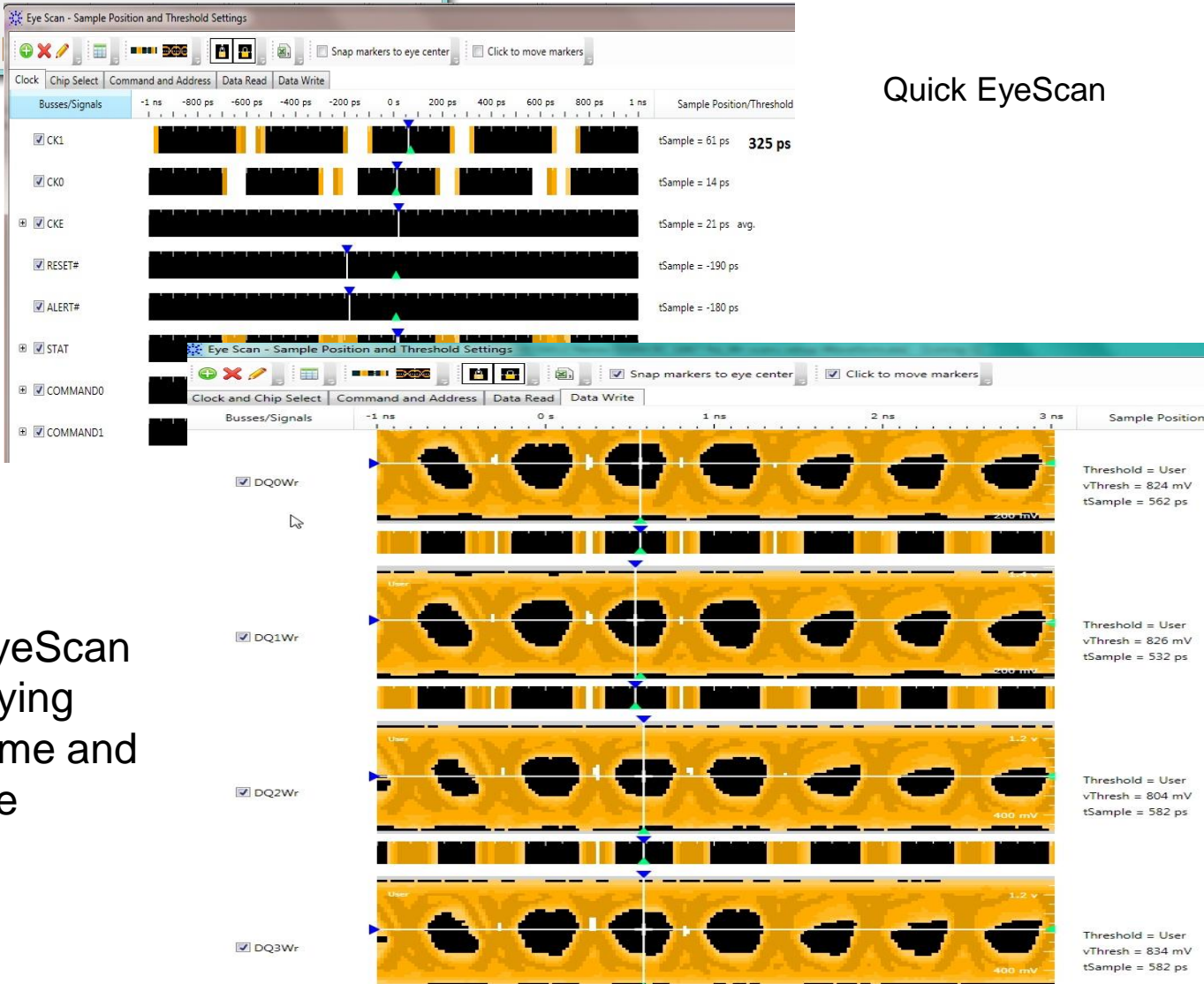## Quick and Accurate Setup with Keysight EyeScan technology

Quickly gain signal integrity insight with Keysight EyeScan technology. As timing and voltage margins continue to shrink, confidence in signal integrity becomes an increasingly vital requirement

of the design verification process. EyeScan lets you quickly acquire comprehensive signal integrity information on the DDR4 bus in your design, and can provide measurements with 5 ps of resolution.

The Logic Analyzer Workspace

User Input for Protocol Decode

Quick EyeScan

Full EyeScan
by varying
both time and
voltage

Ordering Information

FS2520 – DDR4 DIMM Interposer for use with 3 U4164A Keysight Logic Analyzer modules

Software for the FS2520:
B4126B - Keysight provides the Configuration files for both Timing and State modes of analysis and Protocol Decoder software that runs on the Keysight logic analyzer

Keysight Logic Analyzer Requirements

The FS2520 requires
- 1 ea M9505A five-slot AXIe chassis
- 3 ea U4164A 136-channel Logic Analyzer Modules

M9505A

U4164

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