

DDR4 DIMM Interposer

For use with Agilent Logic Analyzers

FuturePlus Systems

Power Tools For Bus Analysis

NEW

- DDR4 2400 MT/s bus analysis
- Used with Agilent U4154A logic analyzer
- Includes protocol-decode software, probe configuration software, and automatic logic analyzer configuration software
- Interposer design does not consume a slot
- Includes Clock Qualifier feature if needed to allow accurate testing in 2 rank systems



FS2501B DDR4 DIMM 2400 Interposer

Key Features

- Quick and easy connection between the DDR4 DIMM SDRAM memory bus connector and Agilent logic analyzers
- Complete and accurate 2400 MT/s state and timing analysis up to 12.5 GHz
- Compatible with all 284-pin DDR4 SDRAM DIMM's up to 2400 MT/s.
- All signals are probed passively.
- Does not require termination adapters; they are built-in
- Registered, unbuffered, and large register DIMMs are supported.
- Burst sizes of 2, 4, or 8 are supported.
- Monitors writes only, reads only, or writes and reads.
- Quick and easy setup using Agilent Eye Scan with 5 ps resolution

Straightforward, Reliable DDR4 2400 Analysis

The FuturePlus® FS2501B DDR4 DIMM 2400 Interposer provides a mechanical, electrical and software interface between an Agilent logic analyzer and the DDR4 connector. The FS2501 is used to design and debug computer motherboards and DIMM's incorporating DDR4 technology.

Helping you Design Tomorrow's Computers, Today

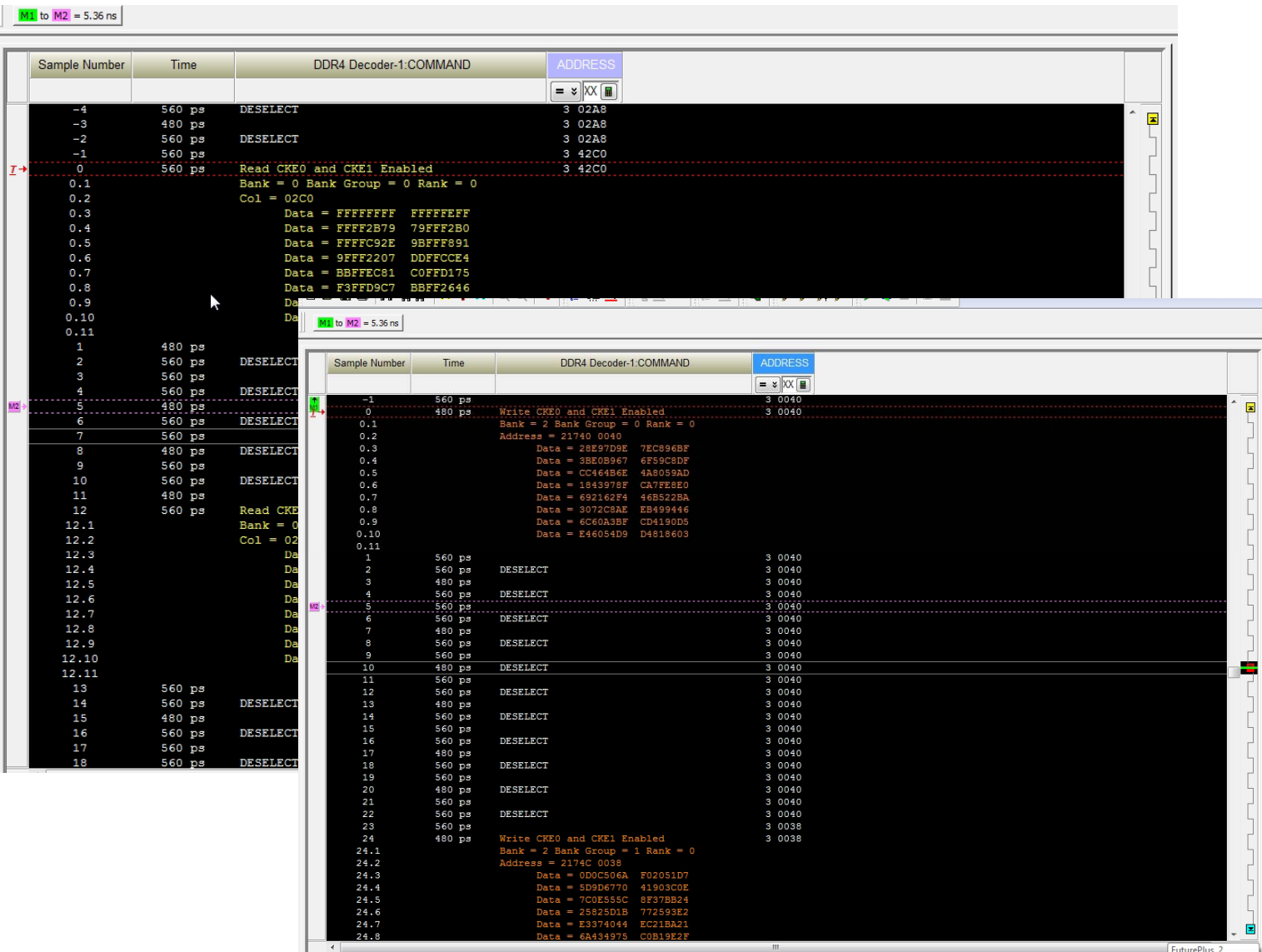
FuturePlus Systems is the technology leader in protocol analysis tools for the computer design industry. Our Interposers and software help you monitor and verify complex activities on your advanced technology computer bus design. FuturePlus systems offerings include bus-analysis solutions for most popular computer buses. Visit www.futureplus.com for more information.



Accurate State Analysis

The FS2501B DDR4 DIMM memory bus interposer brings bus signals to your Agilent logic analyzer via controlled impedance cables for an easy protocol analysis connection while maintaining signal fidelity.

Accurate READ and WRITE State Capture at 2400



The FS2501B protocol-decode software translates acquired signals into easily understood bus transactions, at the full bus speed. The Agilent logic analyzer provides extensive triggering and store qualification features. Depending on the logic analyzer's resources, the FS2501B interposer can be configured to perform State analysis of Reads or Writes, or both Reads and Writes, at 2400 MT/s.

The DDR protocol decode software executes in the logic analyzer and takes user input on system attributes such as Burst length, CAS and Additive Latency, as well as Chip Selects to decode the key DDR bus signals and present a display that lists the transaction type, address, data and command conditions. The software also supports user-defined symbols that can be easily added to the state listing display. User-selectable post-processing filters allow the acquired data to display different types of transactions indifferent colors.

Quick and Accurate Setup With Agilent Eyescan technology

Quickly gain signal integrity insight with Agilent EyeScan technology. As timing and voltage margins continue to shrink, confidence in signal integrity becomes an increasingly vital requirement

of the design verification process. EyeScan lets you quickly acquire comprehensive signal integrity information on the DDR4 bus in your design, and can provide measurements with 5 ps of resolution.

The screenshot displays the Agilent Logic and Protocol Analyzer (LPA) interface. The main workspace shows a configuration tree with the following components:

- Probes: FS2501B (Rev. 1)
- Modules: Slots 1-2 [1] containing a DDR4 Analyzer
- Tools: DDR4 Decoder-1
- Windows: DDR4 Listing, Waveform

The Preferences dialog for the DDR4 Decoder-1 tool is open, showing the following settings:

- Chip Select Used: 2
- Read Latency: 14
- Write Latency: 12
- Command Latency: 0
- Burst Length: 8
- Data Width to Display: All 64 Bits
- Write DBI Enabled: No
- Read DBI Enabled: No
- Address Mirroring: No
- On The Fly:
- Using ECC:
- Row Bits: 18
- Column Bits: 10
- Color coding: GA (orange), BA (red), Row Address (yellow), Column Address (green)
- User Supplied .Net assembly:

The Eye Scan - Sample Position and Threshold Settings window shows the following signals and their parameters:

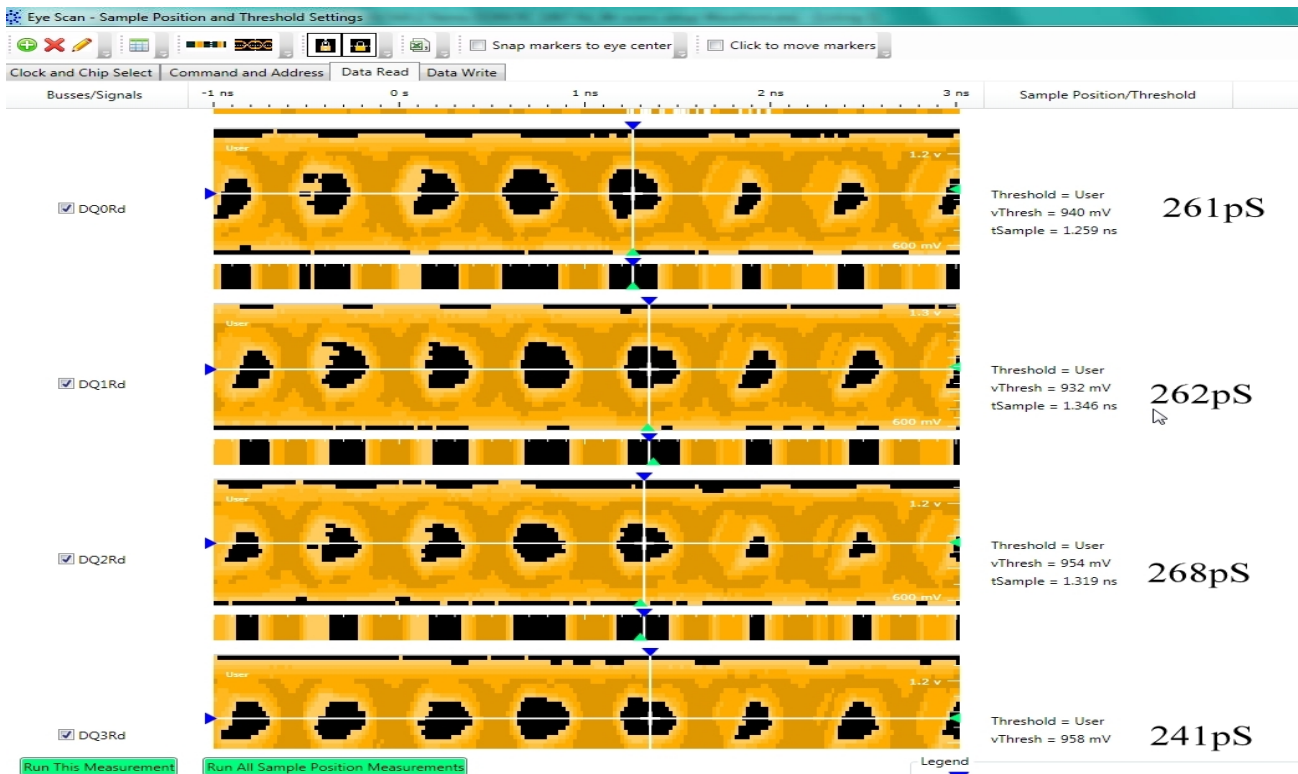
| Signal | tSample |
|----------|------------|
| CK1 | 61 ps |
| CK0 | 14 ps |
| CKE | 21 ps avg. |
| RESET# | -190 ps |
| ALERT# | -180 ps |
| STAT | - |
| COMMAND0 | - |
| COMMAND1 | - |

The detailed Eye Scan window for data buses DQ0Wr, DQ1Wr, DQ2Wr, and DQ3Wr shows the following parameters:

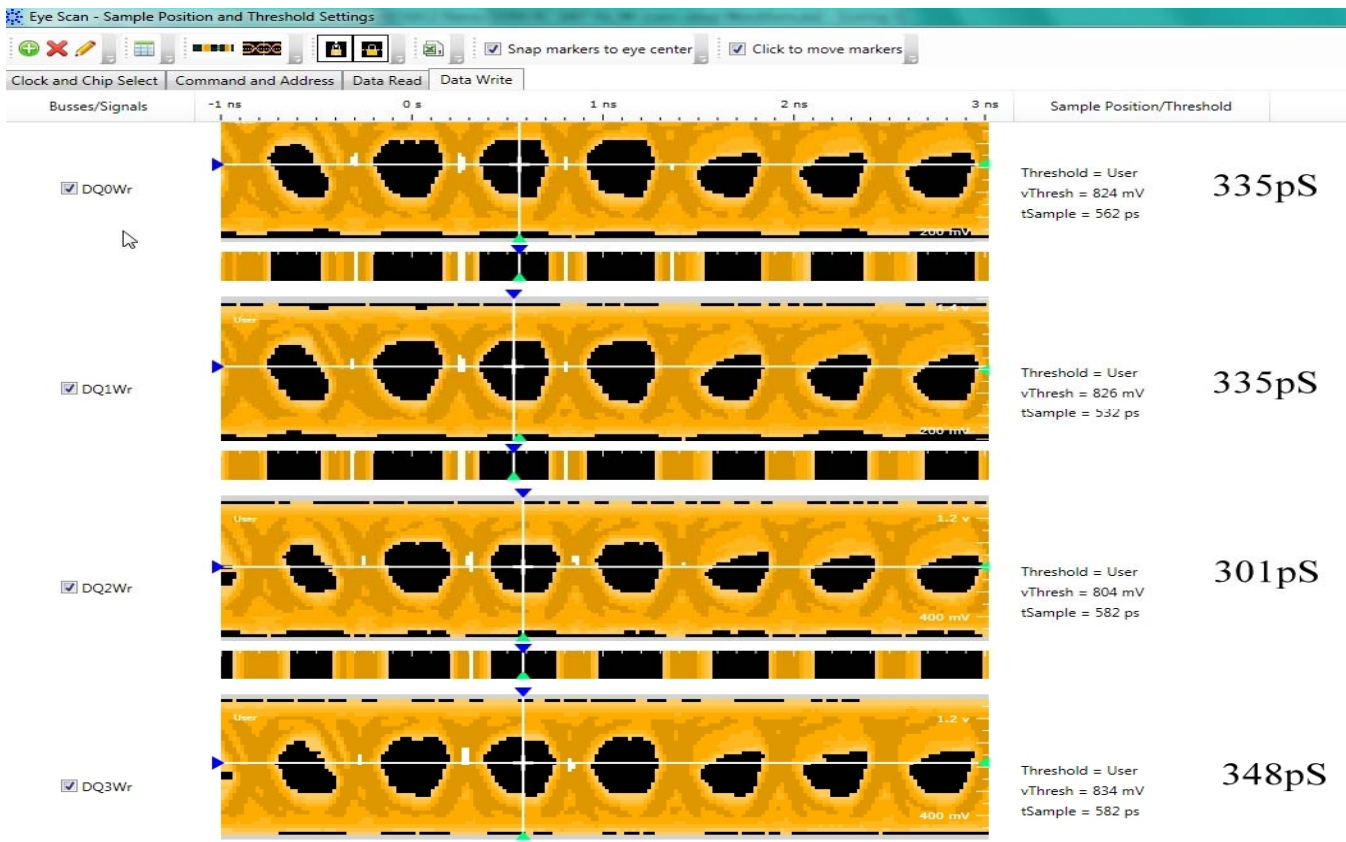
| Signal | Threshold | vThresh | tSample |
|--------|-----------|---------|---------|
| DQ0Wr | User | 824 mV | 562 ps |
| DQ1Wr | User | 826 mV | 532 ps |
| DQ2Wr | User | 804 mV | 582 ps |
| DQ3Wr | User | 834 mV | 582 ps |

Demonstrated 2400 operation

DDR4 READ Eyes from Eyescan Display on the FS2501B



DDR4 WRITE Eyes from Eyescan Display on the FS2501B

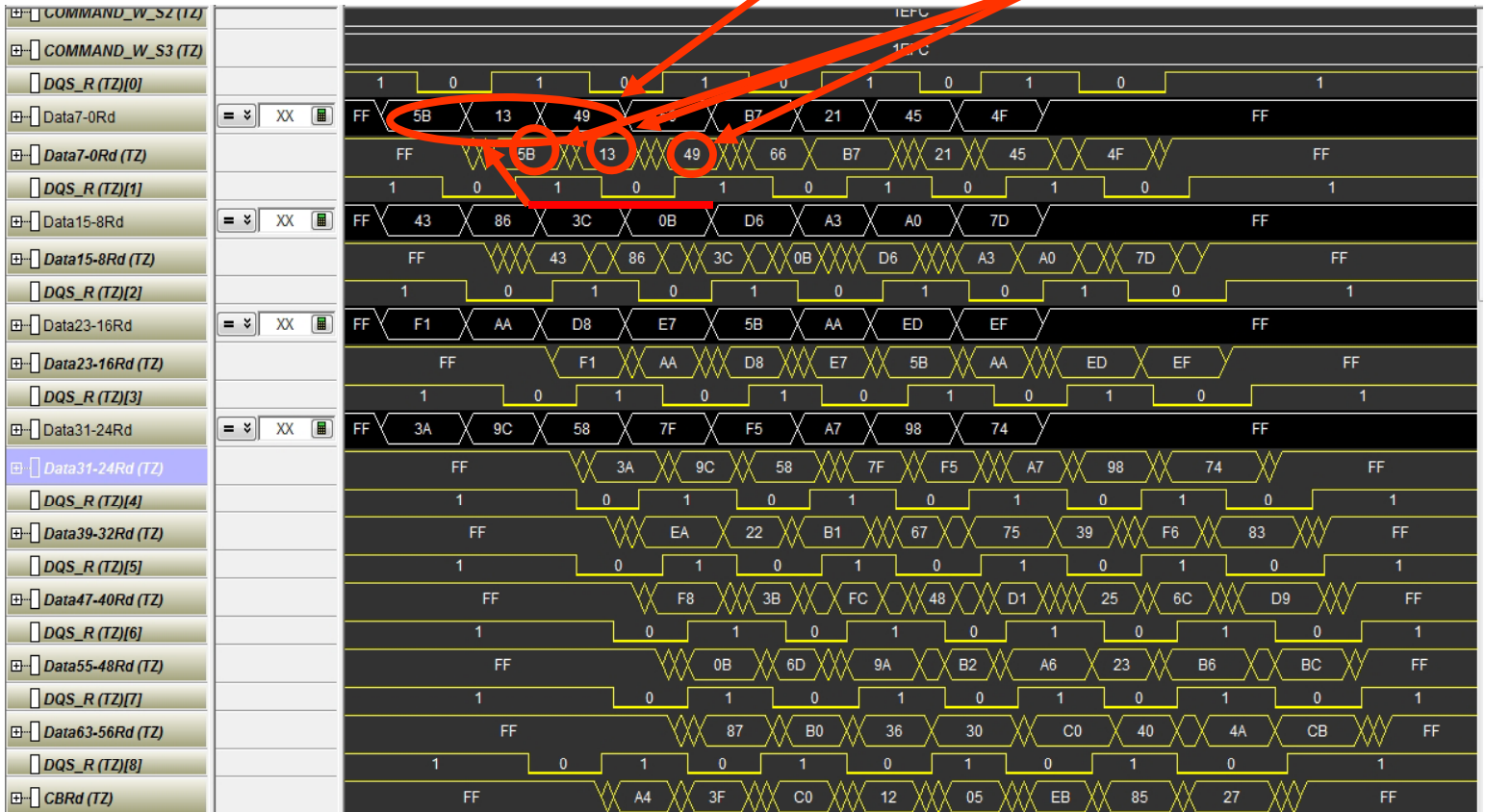


2400 State Capture Verified

DDR4 READ operation

State Capture

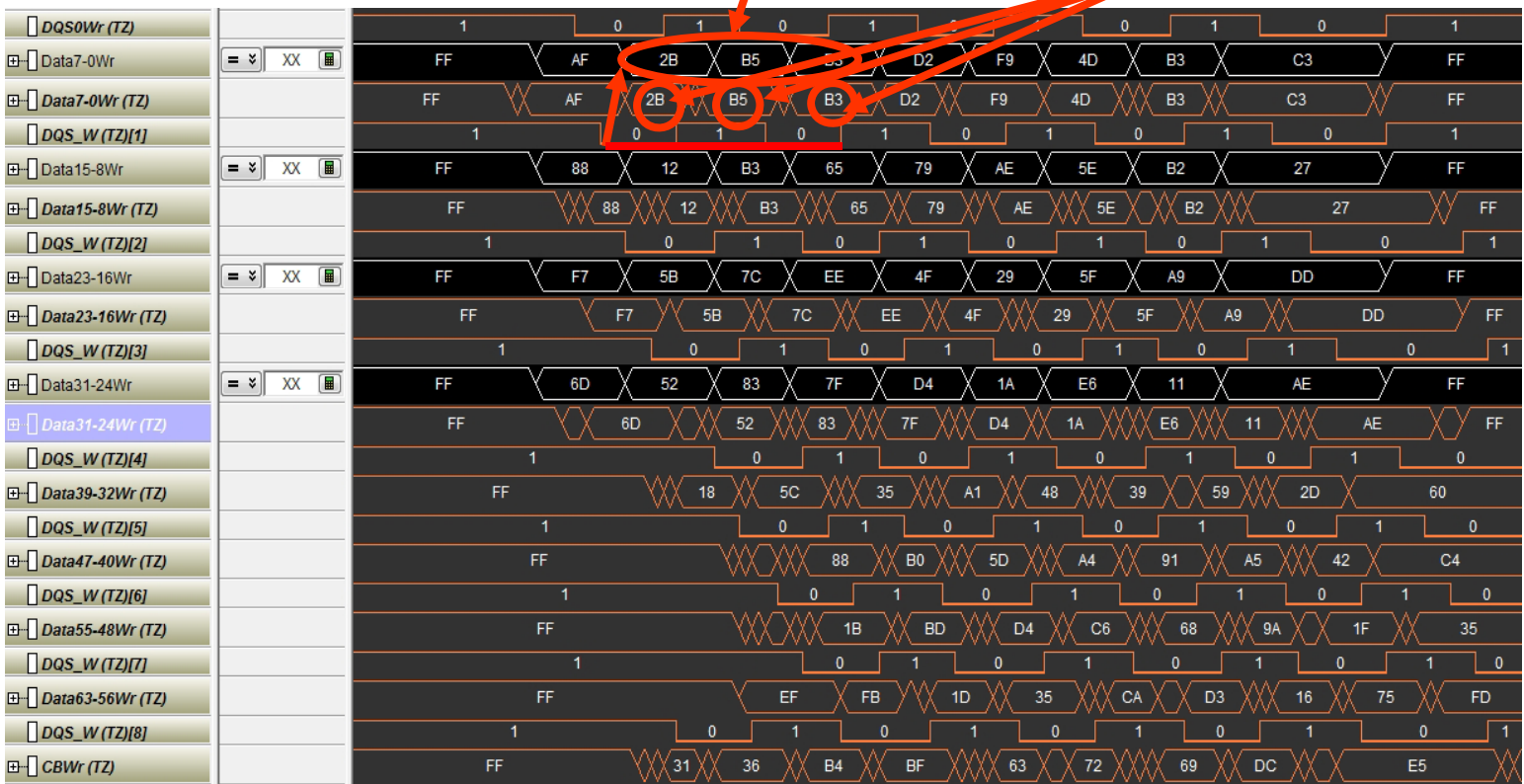
Timing Capture



DDR4 WRITE operation

State Capture

Timing Capture



Ordering Information

FS2501B – DDR4 DIMM Interposer for use with Agilent Logic Analyzers

Software included with the FS2501B:

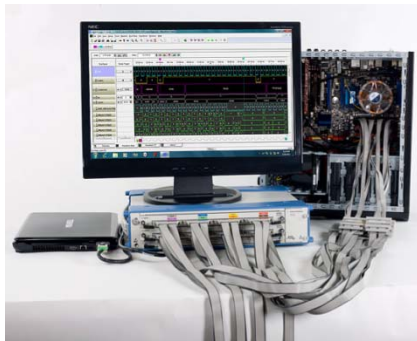
Configuration files for the Agilent logic analyzer

Protocol Decoder software, runs on the Agilent logic analyzer

Agilent Logic Analyzer Requirements

The FS2501B requires

- 1 ea M9502A two-slot AXIe chassis
- 2 ea U4154A 136-channel Logic Analyzer Modules



M9502A



U4154A

FuturePlus Systems Corporation

36 Olde English Road

Bedford, NH 03110

Tel: 603 471-2734

Fax: 603 471-2738

Website: www.futureplus.com