

Linear Pluggable Optics

OIF-CEI 112G Linear Pluggable Optics Validation

Solutions for the Linear Pluggable Optics (LPO) Ecosystem

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Agenda

- **Ecosystem Challenges in DataCenter**
- **Test & Validation Challenges**
- **Keysight Solution for Validating and Testing LPO Interfaces**
- **Contacts**
- **Appendix**

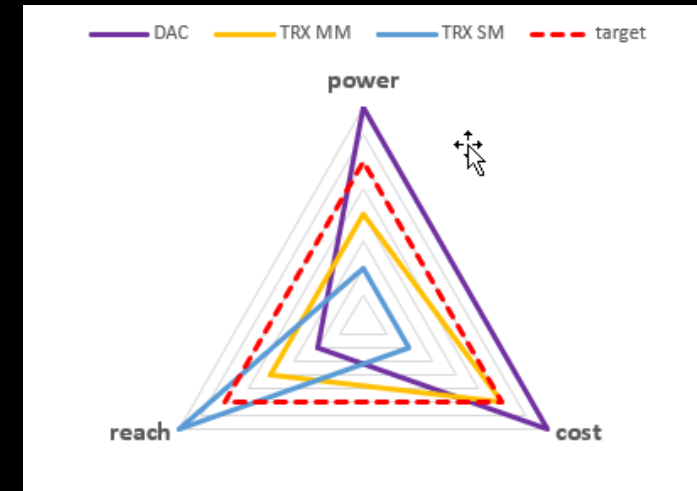
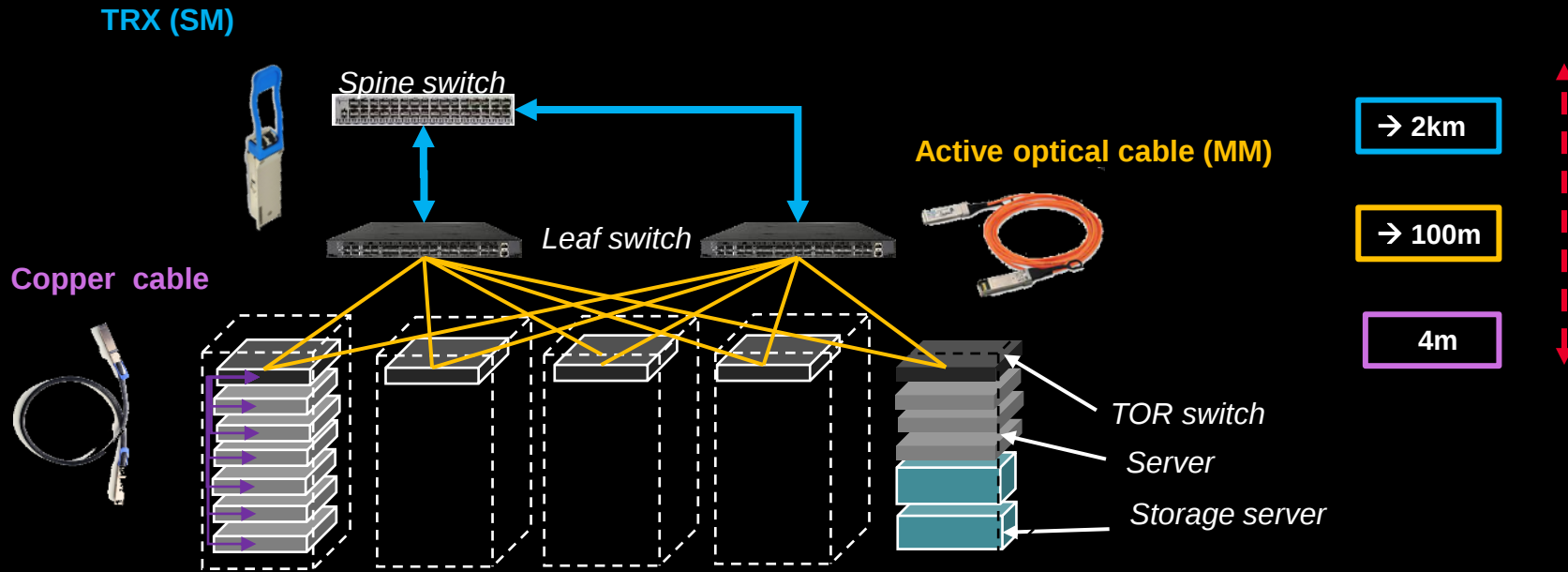


Ecosystem Challenges

The need to reduce latency and power consumption has made the move to linear interfaces an attractive alternative for data center interconnect.

Adapting Hyperscale DC to AI

Requirements for backend (M2M) networking are changing



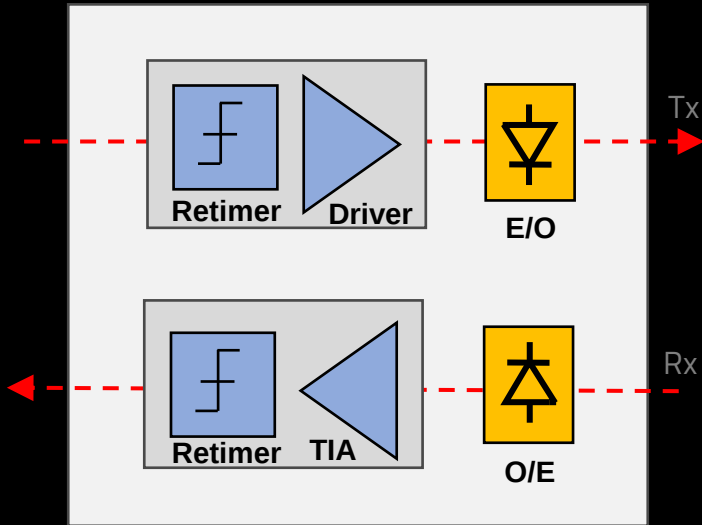
Backend Networking

- More bandwidth (AI workloads 400G SmartNIC card)
- Larger cluster size → longer reaches
- Reduced latency

New type of interconnect is required

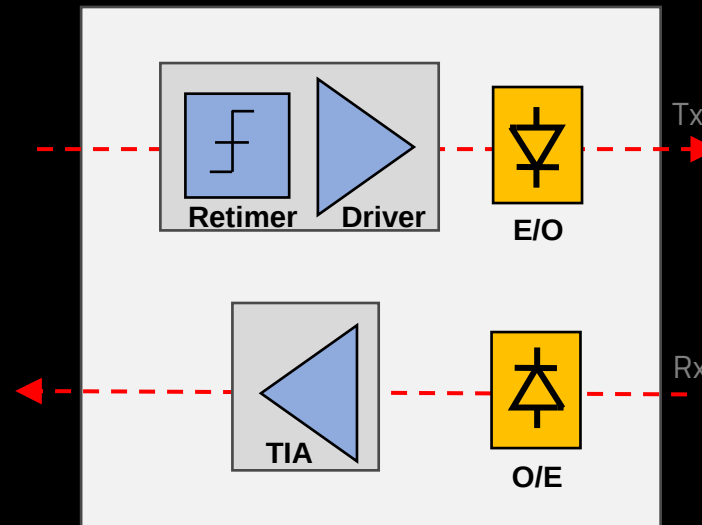
Linear Drive Optics

Types of 100G Modules



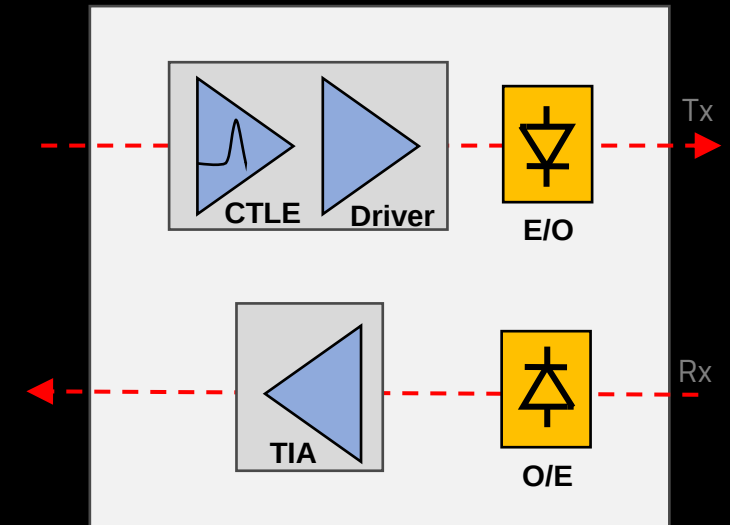
**Full-Retimed Module
(Tx/Rx DSP/CDR)**

- Highest power solution ~17pJ/bit
- Tx and Rx paths both retimed
- Can support higher channel loss on Rx and Tx side compared with LPO
- Noise and crosstalk can be relaxed compared with an LPO module



**Half-Retimed Module
(Tx DSP/CDR)**

- Lower power than full-retimed but higher than LPO ~12pJ/bit
- Tx is retimed, Rx is un-retimed
- Can support higher channel loss than LPO



**Non-Retimed or
LPO/Linear Module
(Analog Driver + TIA only)**

- Lowest power solution ~7pJ/bit
- Requires clean HOST port channels
- Correct host switch equalization is crucial
- Noise and crosstalk accumulation need to be controlled

Linear Drive Optics

Standardization (Oct'24)

LPO-MSA

100G-DR-LPO

Draft Revision 0.6

Specification for
100 Gb/s per Lane Linear Pluggable Optics
Single-Mode Optical Fiber Transmission

LPO MSA Member Companies	
1-Via	Inpho
Accelink	Intel
Adtran	Jabil
AMD	Juniper
Arista	Keysight
Broadcom	Lumentum
Bytedance	Luxshare
CIG	Macom
Cisco	Multilane
Coherent	New Photonics
Color Chip	Nubis
Dell	NVIDIA
Eoptolink	Omniva
Exfo	O-Net
Fast Photonics	Semtech
Formica OptoElectronics	Source Photonics
HG Genuine	TeraSignal
Hisense	Wilder Technologies
Huawei	
Hyperphotonics	

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LPO MSA spec rev 1.0 expected Feb'26

OIF

Implementation Agreement OIF-CEI-5.2

Common Electrical I/O (CEI)

Contribution Number: oif2021.405.10

Working Group: Physical Link Layer (PLL)

Title: CEI-112G-LINEAR-PAM4

Source: Tom Palkert
Macom
tom.palkert@macom.com

Contributor(s): Rich Mellitz, Brandon Gore, Samtec Corporation
Ryan Latchman, Macom

Date: September 3, 2024

Abstract: CEI-112G-LINEAR-PAM4 specifies a 112 Gb/s chip-to-module, near package or co-packaged PAM4 electrical interface for use in the range 36 to 56 Gsym/s with up to 13 dB loss at the Nyquist frequency, including one connector. This specification removes the requirement for a DSP/re-timer in the module and instead uses the strong equalizer capabilities of the host ASIC.

This document will be added as a new clause in a future revision of CEI 1A. References to other clauses are consistent with OIF-CEI-5.3 1A.

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Optical Internetworking Forum - Clause 29: CEI-112G-LINEAR-PAM4

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OIF-CEI 112G linear specs are final

OIF CEI-224G New Project Starts

CEI-224G-XSR

2.5D Chip-to-Chip

Chip to Co-Pkg Optics Engine

Up to 50mm package substrate
1e-15 or lower (FEC is allowed)

CEI-224G-VSR

Chip to Module

Plastic Optics

200mm of host, 20mm of module
1 connector
1e-15 or lower (FEC is allowed)

CEI-224G-MR

Chip to Chip

Chip-to-Chip & Midplane Applications

500mm of reach
1 connector
1e-15 or lower (FEC is allowed)

CEI-224G-LR

Chip to Chip

Backplane or Passive Copper Cable

1000mm of host and daughter cards
2 connectors
1e-15 or lower (FEC is allowed)

CEI-212G-Linear¹

Chip to Co-Pkg/Near-Pkg Optics Engine

Non-retimed optics to save power and cost
Without DSP/SERDES in Optical Module
1e-15 or lower (FEC is allowed)

- CEI-224G LR Draft Specification is currently in review for OIF members
- New Projects started at OIF Q1 2025 meeting
- One-Series core might not be able to cover multiple applications from XSR to Linear
- For short reach applications, simpler and lower power equalizations are desired
- Retimed 7x Linear Rx Specs CEI Project Start in OIF Q1 2024 meeting covering 200G/lane over 500m SMF link

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Optical Internetworking Forum - Clause 29: CEI-112G-LINEAR-PAM4

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OIF-CEI 224G linear project (proposal stage)

Keysight - Testing LPO Interfaces

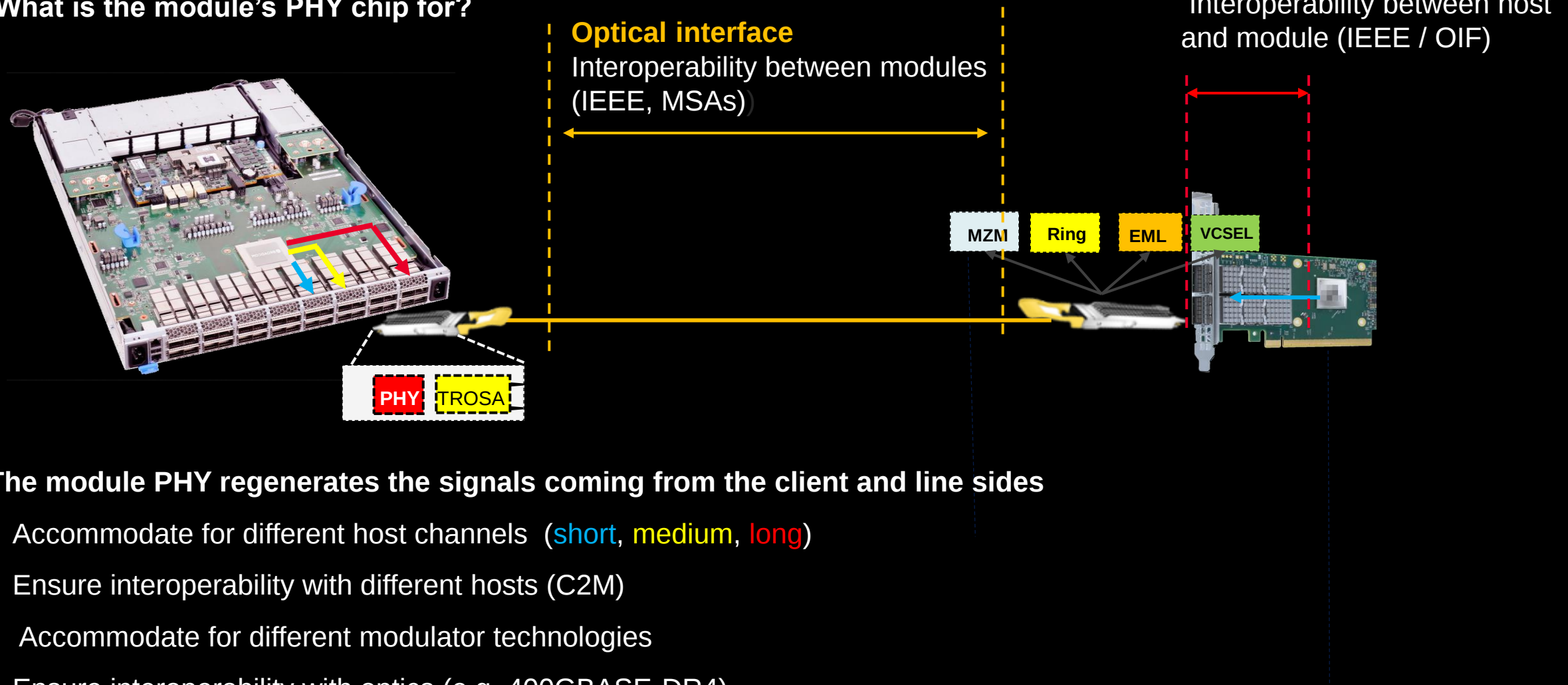
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A multi-source supply chain strategy requires interoperability

Test and Validation Challenges

High-speed link in the data-center

What is the module's PHY chip for?

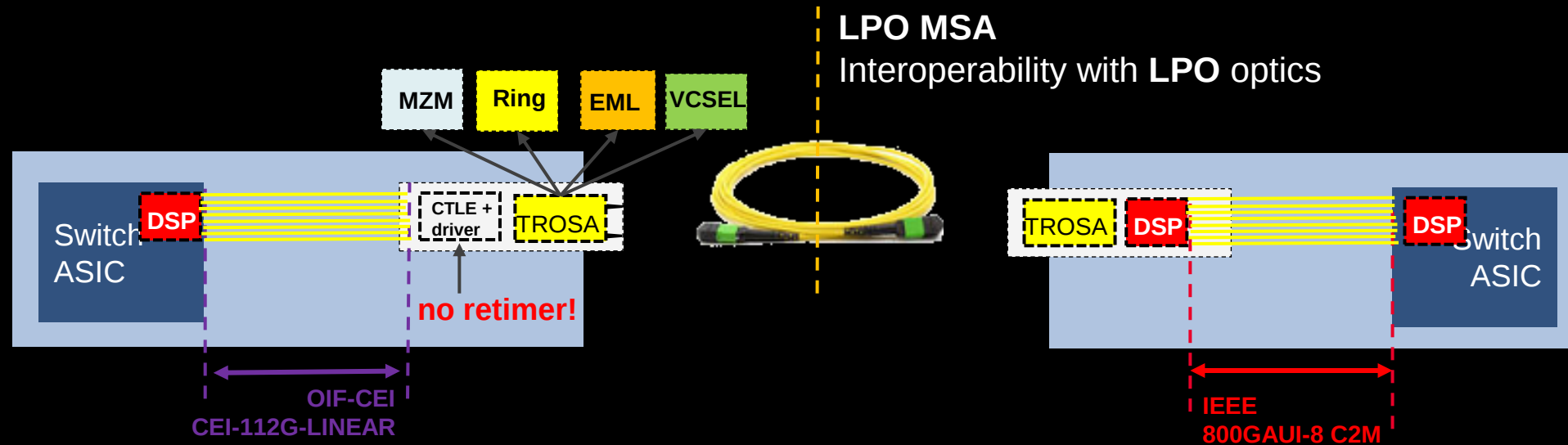


The module PHY regenerates the signals coming from the client and line sides

- Accommodate for different host channels (short, medium, long)
- Ensure interoperability with different hosts (C2M)
- Accommodate for different modulator technologies
- Ensure interoperability with optics (e.g. 400GBASE-DR4)

Linear Pluggable Optics

Multiple challenges



Challenge #1: Validate **host** independently from module

- Tx: accommodate different modulator technologies & PCB channels
- Rx: Accommodate for highly distorted (different kinds of impairments accumulated over the link)

→ T&M equipment to emulate a reference module

Challenge #2: Validate module independently from host

- Ensures interoperability with other LPO optics (but potentially also with legacy “retimed” modules)
- Validate module output independently from the host

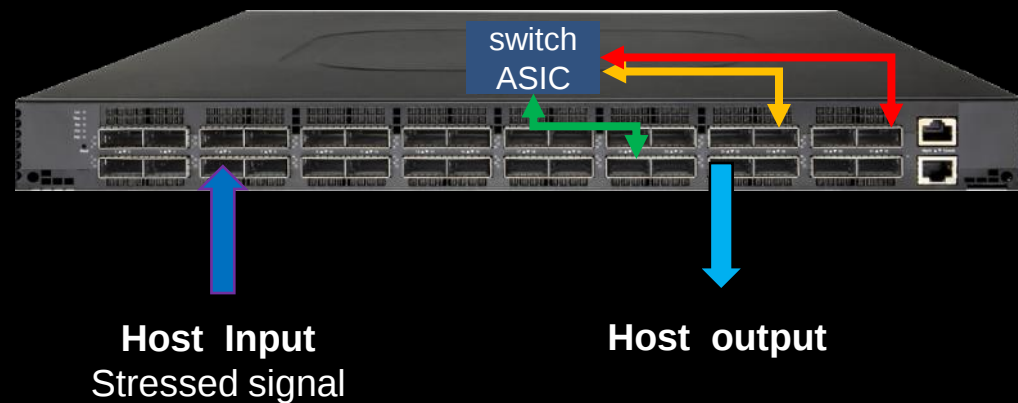
→ T&M equipment to emulate a reference host

Validating and Testing LPO interfaces

Overview

Validating switches & NIC host chips

- Output and Input test for all ports
- Standards distinguishes **short**, **medium** and **long** channels



Validating LPO modules

- Module input for **short**, **medium** and **long** host channel
- Module output applying a worst-case (stressed) optical signal applied

Module Input Test

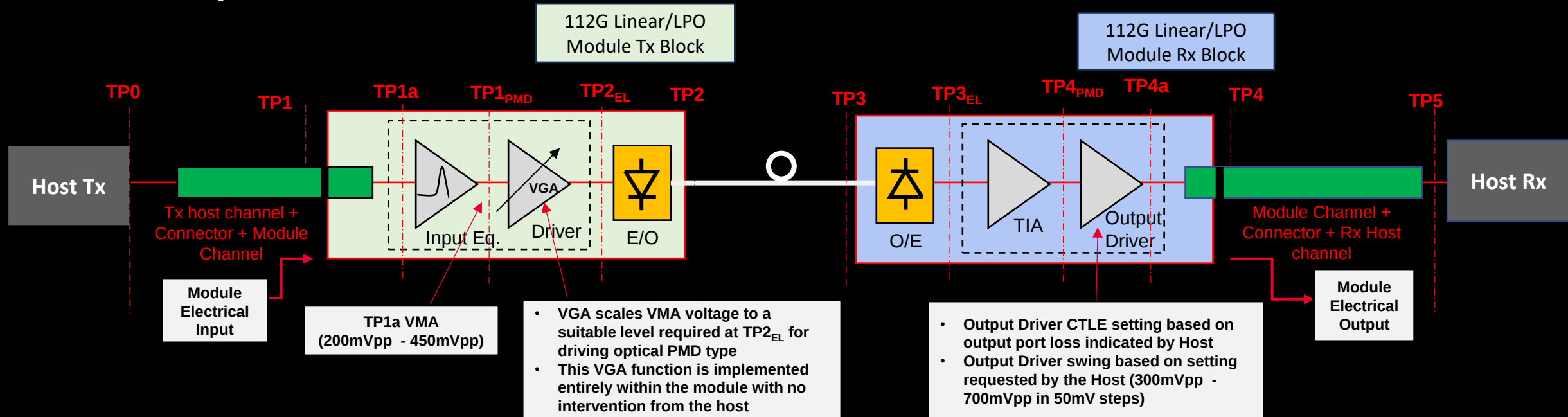


Module Output Test



Validating and Testing LPO interfaces

Linear/LPO System Overview



- HOST Tx FIR and HOST Rx do majority of equalization
 - Limited equalization in module driver and TIA with Analog CTLE
 - Tx TP0-TP1a equalization carried out by host Tx FIR in combination with module input CTLE
 - Rx equalization at TP4/TP5 carried out by host Rx CTLE/FFE/DFE equalizer

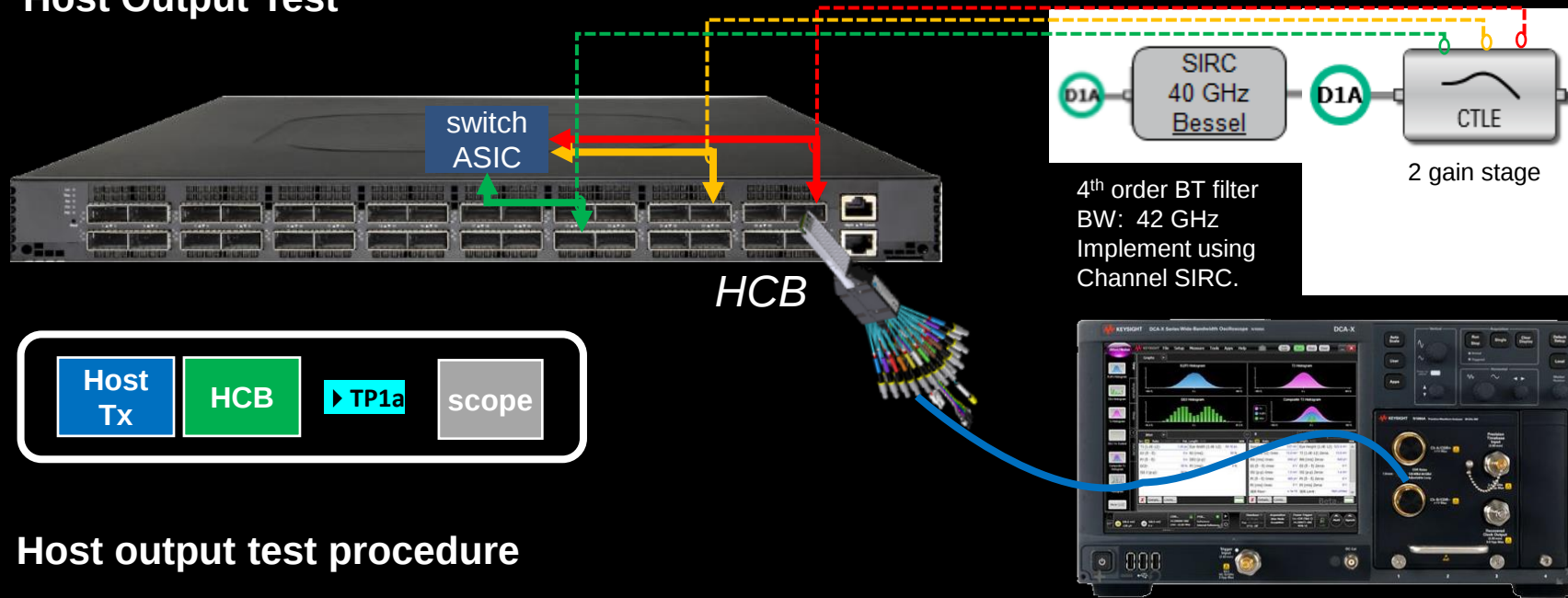
TDECQ : Established Optical Metrics

- **TDECQ:** *TDECQ is a penalty operation that calculates how much noise can be added by an ideal receiver to the signal compared to an ideal (unequalized, noiseless) transmitter. $TDECQ (dB) = 10 \log (OMA_{TDECQ} / (6 \cdot Q_t \cdot R))$*
- **OMA:** *Optical Modulation Amplitude, The measure of the difference in the optical power between outer levels of a PAM4 signal.*
- **CEQ:** *The Ceq noise measurement evaluates the noise gain introduced by the TDECQ equalizer. Ceq is expressed as: $Ceq(dB) = 10 \log_{10}(\text{Noise-out} / \text{Noise-in})$*

EECQ : Recently Introduced Electrical Metrics

- **EECQ:** *Introduced in [CONTRIBUTION OIF2021.592.02](#): Similar to the TDECQ operation but offers insights into signal quality in the context of your expected reference equalizer and physical channels. $EECQ(dB) = 20 \log (VMA_{EECQ} / (6 \cdot Q_t \cdot R))$*
 - **VMA:** *Voltage Modulation Amplitude, The measure of the difference between the voltages in the outer levels of a PAM4 signal.*
- CEEQ:** *Introduced in [CONTRIBUTION oif2024.243.03](#): The Ceeq operation calculates the gain of the input noise excluding the CTLE from the calculation meaning that a set of FFE taps produces a consistent Ceeq regardless of CTLE settings. Ceeq is expressed as: $Ceeq(dB) = 20 \log_{10}(\text{Noise-out} / \text{Noise-in})$*

Host Output Test



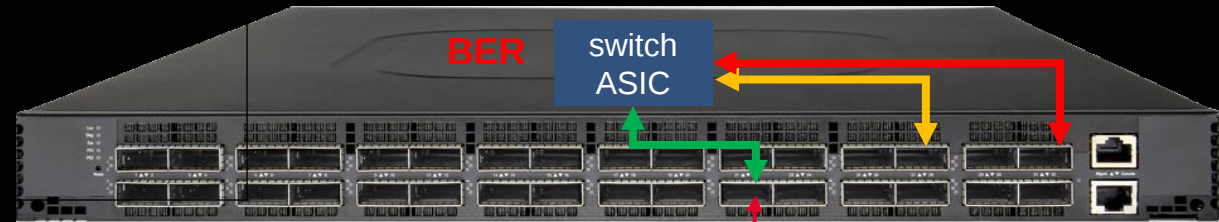
Host output test procedure

- Set the ref. Rx CTLE according to the channel loss
- Find the optimal Tx settings using a TDECQ equalizer to emulate TX FIR
- Measure **EECQ**, **Ceq** and **VMA** using optimized Tx FIR and reference receiver (PRBS13Q)

Host Testing

Host Input Test

BERT



HCB

▶ TP4a

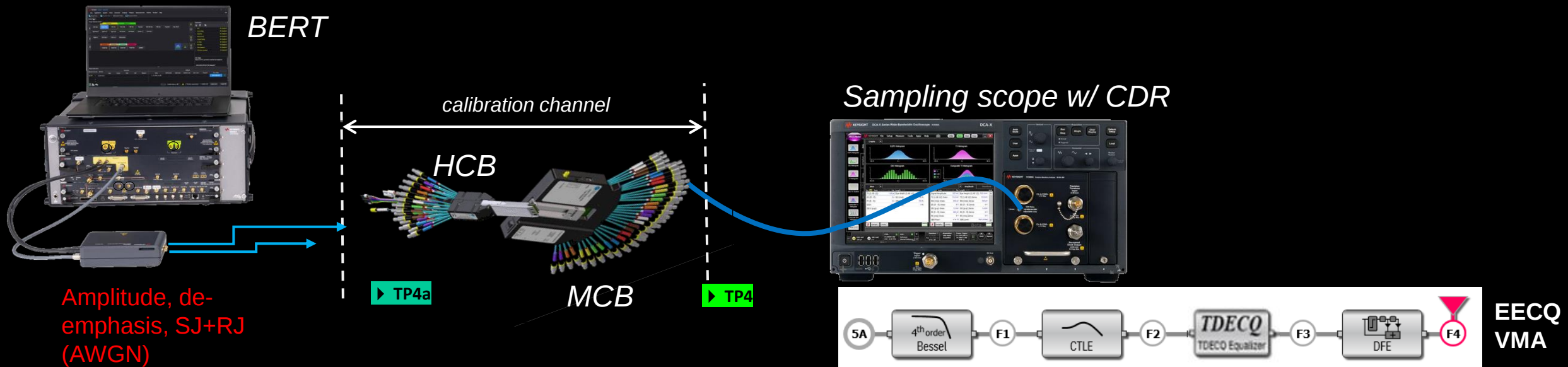
Test procedure

- Calibrate stress signal (next slide)
- Apply stressed **PRBS31Q** pattern (resp. FEC encoded scrambled idle)
- Measure **BER** on the host (resp. **FLR** or **FEC block stats**)



Host Testing

Host Input Test - Calibration



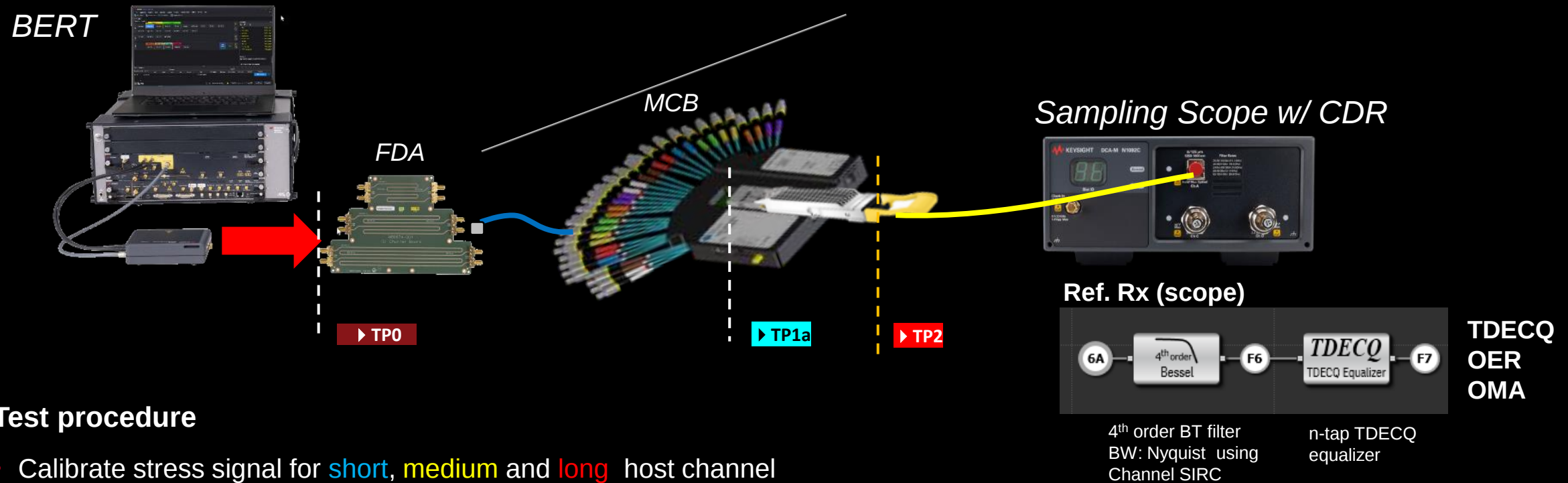
Calibration procedure (e.g. OIF-CEI 112G linear*)

- Optimize reference receiver (RPBS13Q)
- Adjust PG amplitude RJ to meet VMA and EECQ targets

* stress signal calibration For OIF.CEI 112G linear and LPO MSA are slightly different – refer to the latest specification documents

Validating LPO Modules

Module Input Test



Test procedure

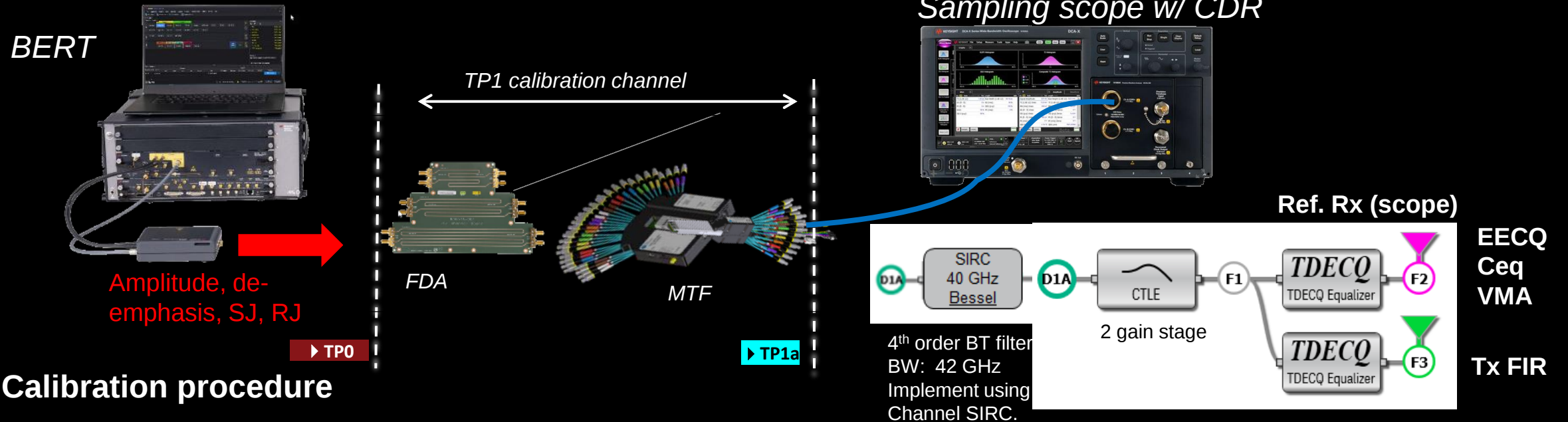
- Calibrate stress signal for **short**, **medium** and **long** host channel (next slide)
- Measure **TDECQ**, **OMA**, **OER**, **Ceq**, over- & undershoot at TP2 using reference receiver*

* Reference receiver and limits are different for IEEE and LPO MSA



Validating LPO Modules

Module Input Test - Calibration



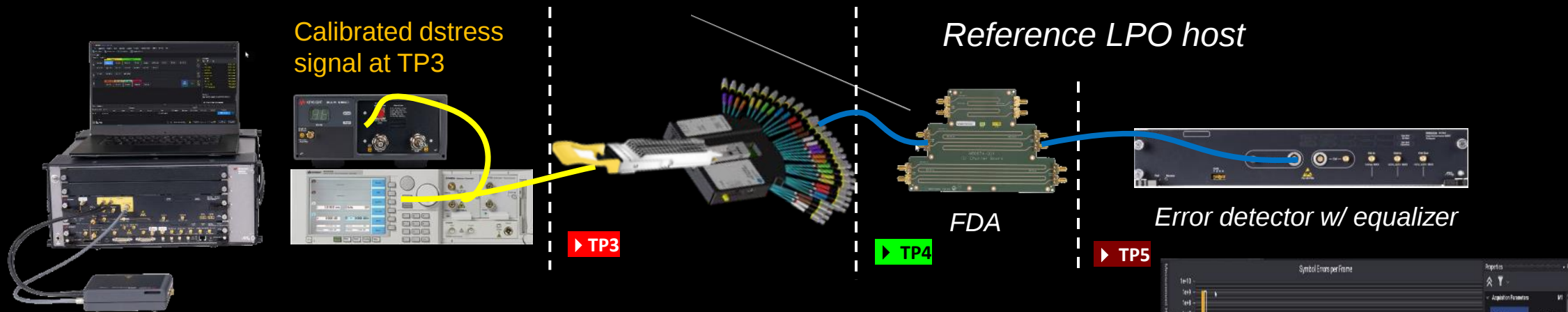
Calibration procedure

- FDA used to emulate three different host channels (short, medium and long)
- Set the ref. Rx CTLE according to the channel loss
- Set PG FIR optimal **EECQ** & **CEEQ** at TP1a
- Tune PG amplitude & random jitter to meet **EECQ** and **VMA** limits (PRBS13Q)



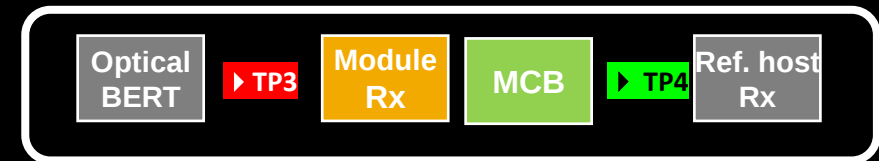
Validating LPO Modules

Module output test – TP5 (LPO MSA)



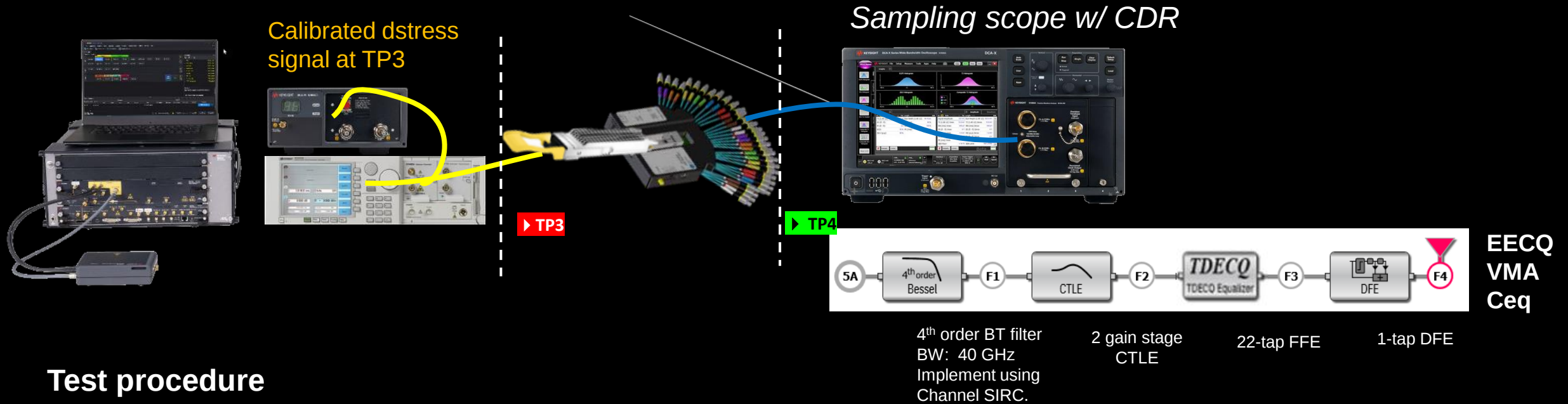
Test procedure

- Calibrate* stress signal TDECQ, OER, OMA at TP3 (SSPRQ)
- Measure BER or FEC-stats at TP5 (PRBS31Q or FEC-scrambled idle)



Validating LPO Modules

Module output test – TP4 (OIF_CEI & LPO MSA)



Test procedure

- Calibrate* stress signal TDECQ, OER, OMA at TP3 (SSPRQ)
- Set the ref. Rx CTLE according to the channel loss
- Co-optimize 22-Tap CTLE and 1-Tap FFE (see next slide)
- Measure EECQ, VMA, Ceq at TP4 (PRBS13Q)

* calibration slightly different between IEEE and LPO-MSA



Testing and Validating LPO interfaces

Keysight solution for validating and testing
LPO interfaces

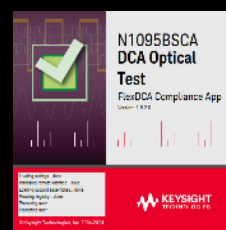
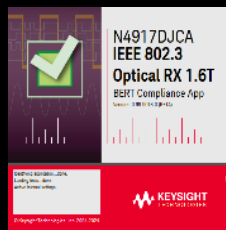
Keysight Solution for Validating and Testing LPO Interfaces

LPO module

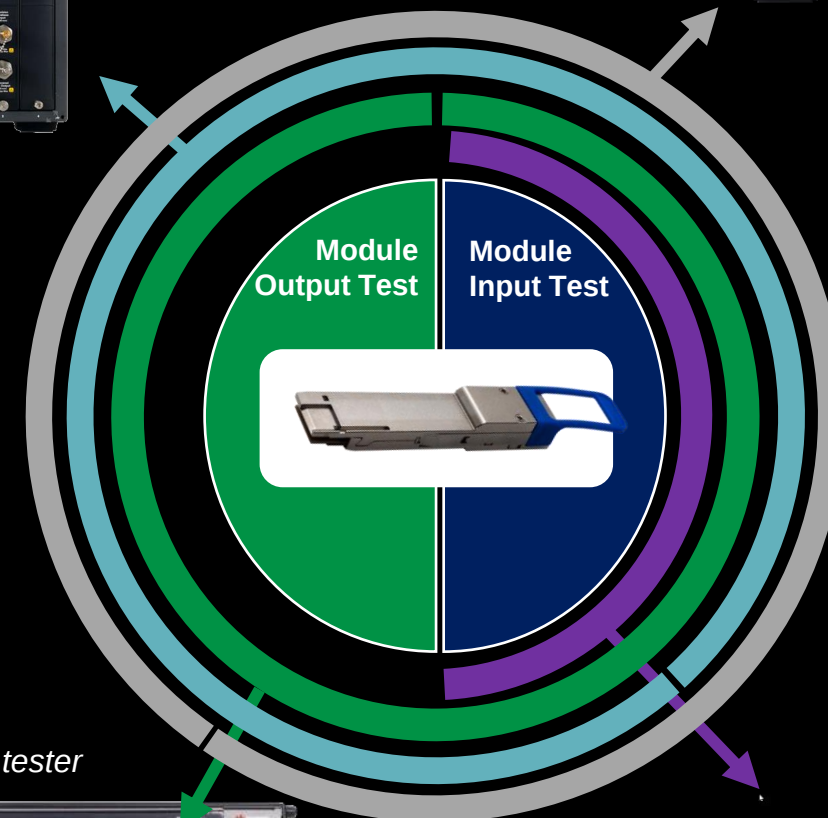
N1060A
85GHz sampling scope w/
integrated 64Gbd CDR



N1092x
Optical sampling oscilloscope w/
64Gbd integrated CDR



SW	Description	Interface
N4917BSCB N4917DJCA	Optical RX Test for IEEE 802.3bs/cd	Module Input Test
N109212CA*	El. TX Test for OIF-CEI 112G Linear	
N1010A	FlexDCA	Module Output Test
N109212CA*	Electrical TX Test for OIF-CEI 112G Linear	
N1095BSCA	Optical TX Test for IEEE 802.3bs/cd	



M8050A
Bit error rate tester

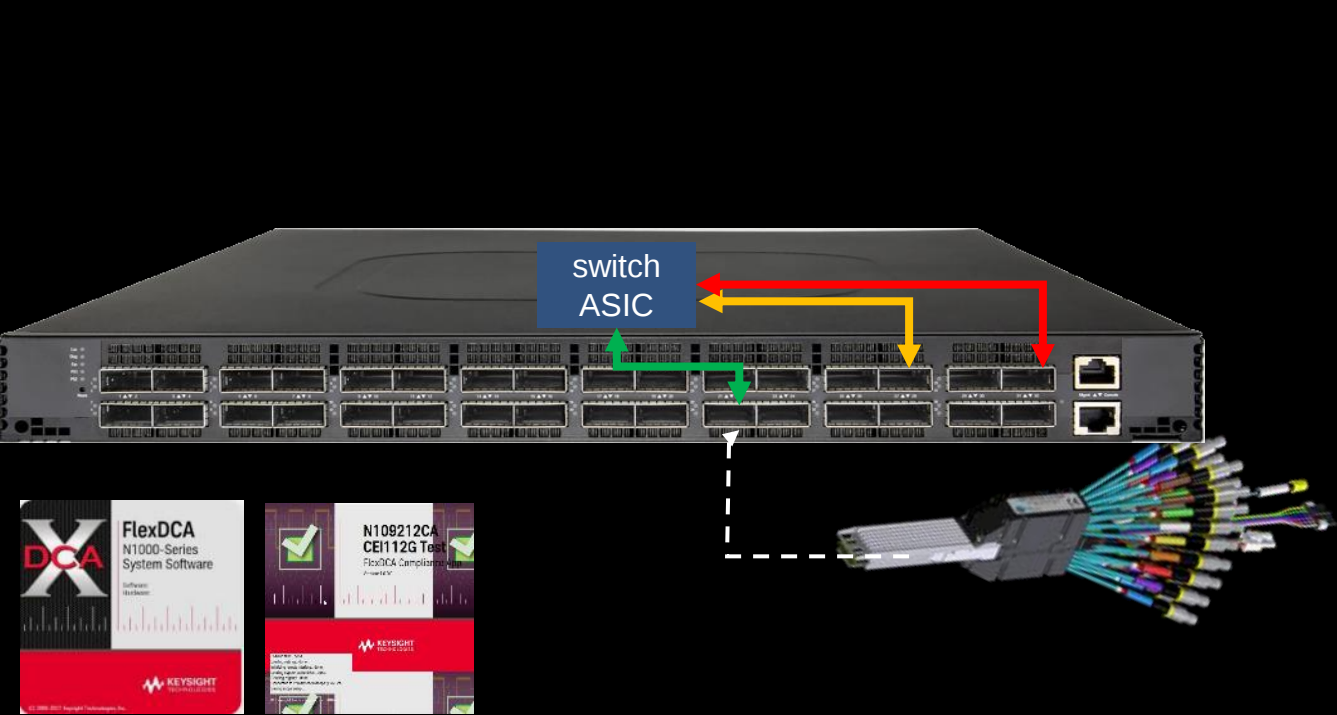


N7718C
Optical reference transmitter

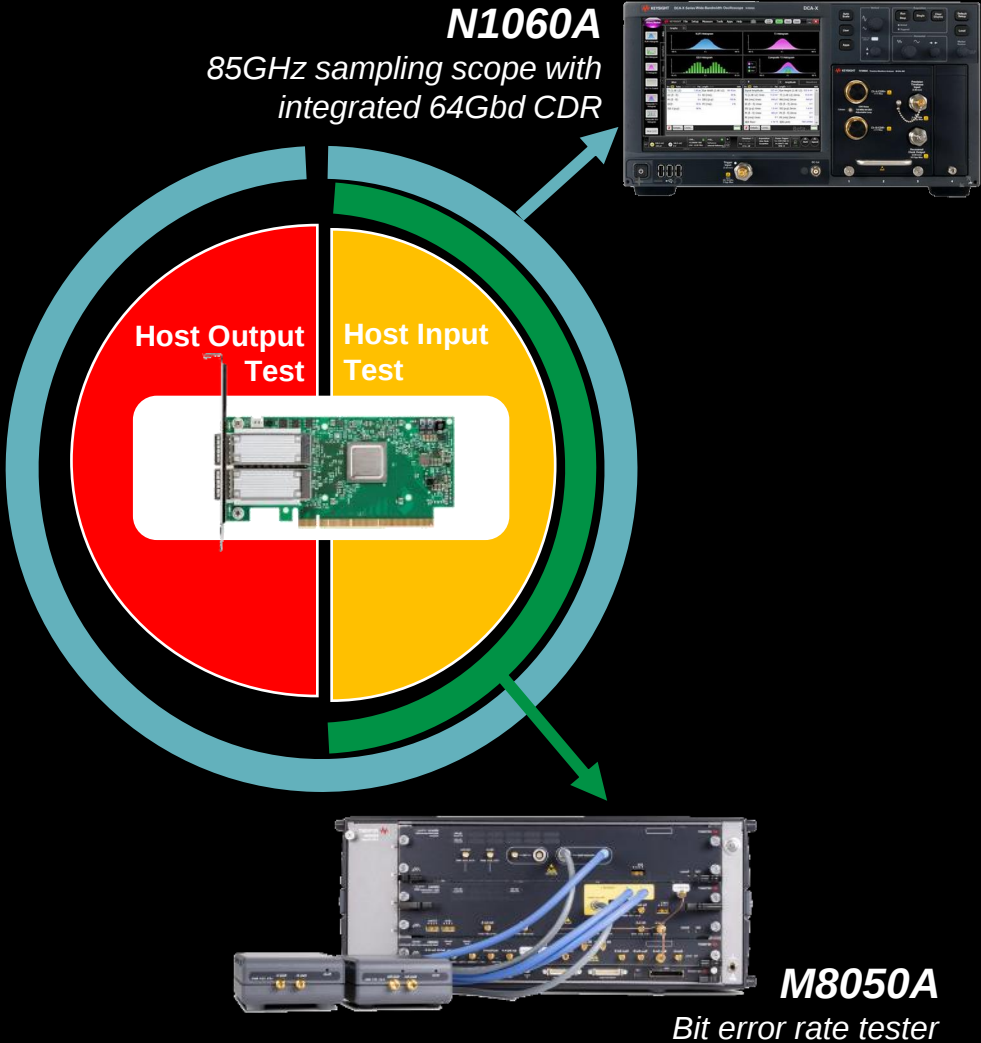


Keysight Solution for Validating and Testing LPO Interfaces

LPO-capable Host

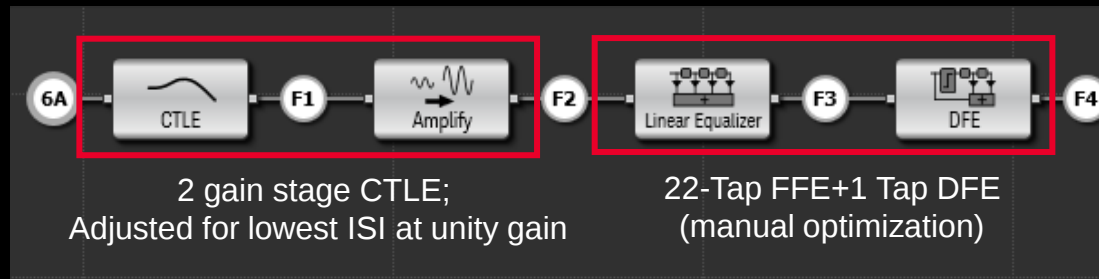


SW	Description	Interface
N1010A	FlexDCA	Host Output Test
N109212CA	Electrical TX Test for OIF-CEI 112G on roadmap	Host Input Test



Keysight Solution for Validating and Testing LPO Interfaces

FFE & DFE co-optimization

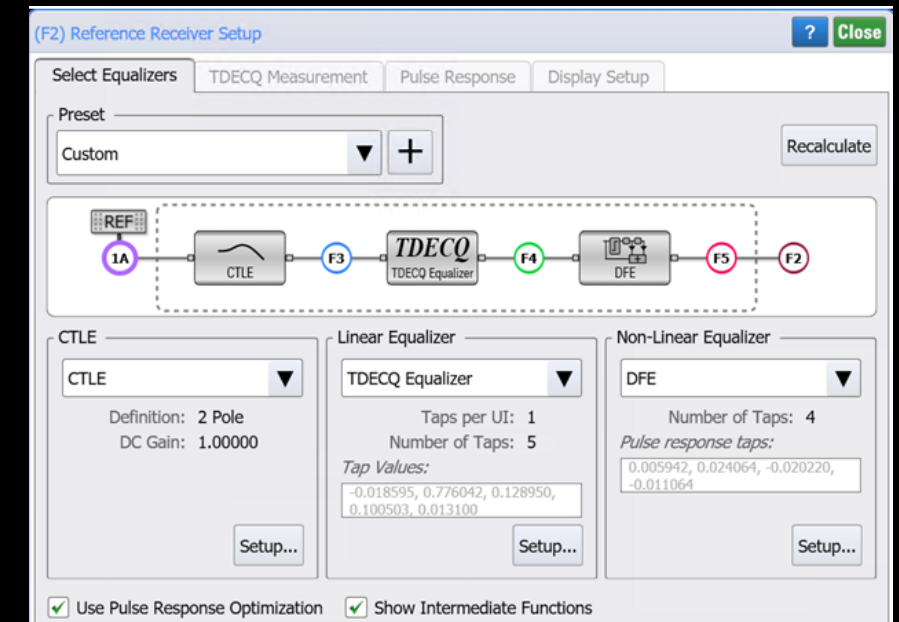


Legacy equalizer

- Manual correction for CTLE gain
- Independent optimization of FIR and DFE
- Leverage of COM tool is complex (pulse response, noise level)

22-tap FFE

1-tap DFE



Reference receiver

- Flexible structure
- Joint optimization FFE and DFE taps (MMSE)
- Pre-defined settings

LPO Module Validation Solution

Module Output



M8050A

N1060A



TP1/TP5

New Tx FIR must be tuned
BER or FEC margin



test signal

loopback

800GAUI-8
MCB

QSFP-DD
OSFP

TP1a/TP4

new EECQ ("electrical TDECQ")
Ceq, SNDR, Jitter, Linearity
new reference equalizer structure

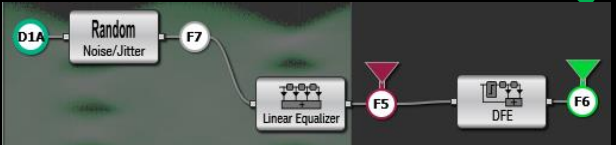
New tune driver gain
and CTLE gain

TP2/TP3

TDECQ, OMA,
ER, RLM, Ceq

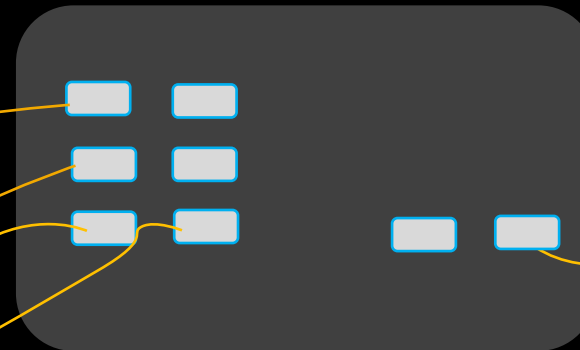


N1092A



Keysight solution LPO interfaces

LPO module – Fully automated functional testing (MFG)



Optical switch
(Keysight or 3rd party)

4-port 800G Interconnect Tester ([specs](#))

- DAC, ACC, AEC, retimed and LPO modules
- PRBS & FEC statistics, eye analysis
- AN/LT
- 50G & 100G lanes (50GE to 800GE speeds)
- Layer 2-3 Tx/Rx and capture traffic generation
- RoCEv2, and AI traffic generation (optional)



FlexOTO – solution bundle
Automated testing for multiple port devices



LPO Modules Validation Solution

* According to "LPO MSA"

Hardware Overview						
	Model	options	Conformance*		Functional	comments
			TP2	TP4		
M8050A DCA-X	M8050A	-BU2				Can be replaced by M8040A BERT (tbc)
	M8009A	-061/ -0G3	Opt. A	Opt. A	-	
	M8042A	-0G1/-G64/-0G4	Opt. A	Opt. A	-	
	M8043A	-0A1/-A64/-0A3		(x)	-	BERT at TP4 is optional.
	M8058A	-	X	X		32/64GBd remote head
	N1000A	-PLK /-STB	(x)	X	(x)	TP2: DCA-X required for TP1a input signal calibration TP4:
	N1060A	-050/-EVA/-264/PTB/-JSA/-E33	(x)	X	(x)	
DCA-M	N109xA	-IRC/-LOJ/-PLK/-280/-206/-30A or 40A	X	X	X	Support both MM and SM 30A for SM or MM, 40A for SM
	N1077B CDR	-264	X	X	X	Support both MM and SM
SW	N109212CA		-	X	-	OIF-112G-Linear option on roadmap
	N4917BSCB	-	-	Opt. A	-	
	N1095BSCA	-	X	-	X	
Fixture	SP0602A/ SP0606A	-	Opt. A	X	(x)	Wilder OSFP/QSFP-DD 112G MCB



LPO Host Validation Solution

Hardware Overview

** According to OIF-CEI 112G linear*

	Model	option	Conformance*		comment
			TP1a	TP4a	
M8050A	M8009A	-061/ -0G3	-	X	Can be replaced by M8040A BERT (tbc)
	M8042A	-0G1/-G64/-0G1/-0G4	-	X	
DCA-X	N1000A	-PLK /-STB	X	X	
	N1060A	-050/-EVA/-264/PTB/-JSA	X	X	
SW	Tx app	-	X	-	
	Rx app TBD	-	-	X	Not on roadmap (manual calibration)
Fixture	SP0603A / SP0607A	-	X	X	112G HCB from Wilder



Appendix

Keysight Testing LPO Solutions



Keysight solutions for the industry

- ✓ Prototype of novel “EECQ” metric available on FlexDCA
- ✓ N1077B – 64Gbd SM & MM CDR
- ✓ M8050A BERT unmatched performance as “LPO”-compatible host (Tx and Rx)
 - Up to 20dB channel (de)-embedding with M8042A pattern generator
 - Advanced equalization capabilities and sensitivity of M8043A error detector

Keysight participation in industry standards

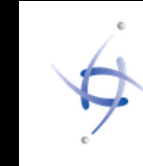
- ✓ OIF CEI-112G-Linear project
 - Technical contributions ([EECQ](#), [overview](#), [Tx test](#))
 - Partnering with industry (MACOM, Eoptolink, Innolight, etc.)



- ✓ LPO MSA member



- ✓ LPO test dry run at InfiniBand Plugfest'24



Public demo

- ✓ **World's first LPO interop demo @ ECOC'23 (OIF-CEI)**
- ✓ **interop demo @OIF-CEI booth @ OFC'24**
 - M8050A as LPO-compatible host Tx & Rx
 - N109x for TP2 optical measurements
 - N1060A for TP1a/TP4 electrical measurements
- ✓ **LPO functional test @ OFCC'24**
 - G800GE as LPO-compatible host Tx & Rx
 - N109x for TP2 optical measurements
 - N1060A for TP1a/TP4 electrical measurements

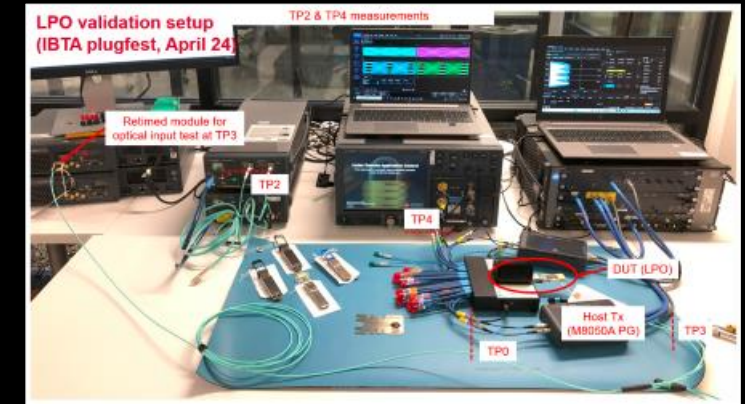
Keysight Testing LPO Solutions



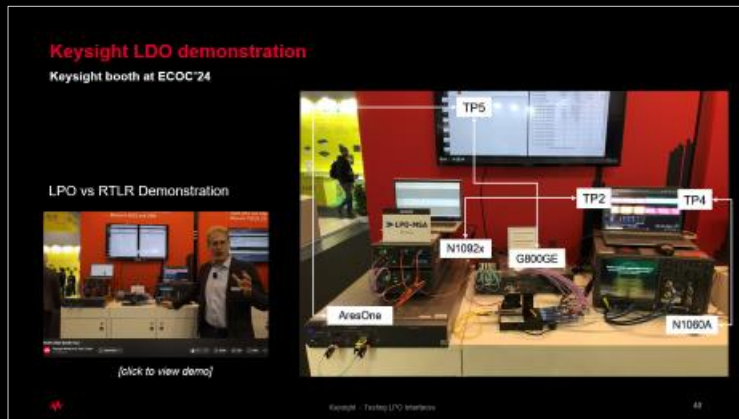
LPO setup in Keysight's lab



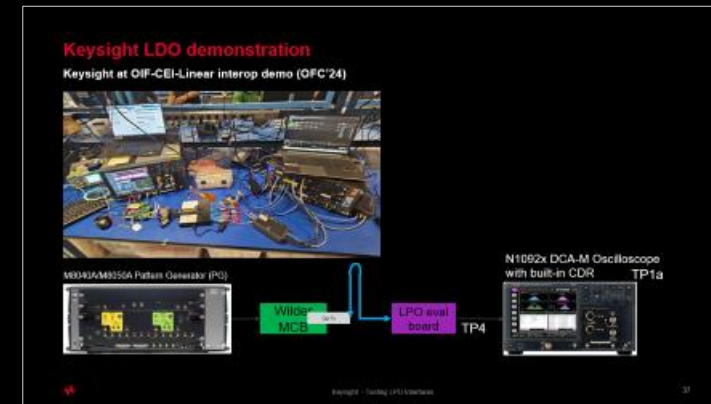
LPO validation demo at OFC'24



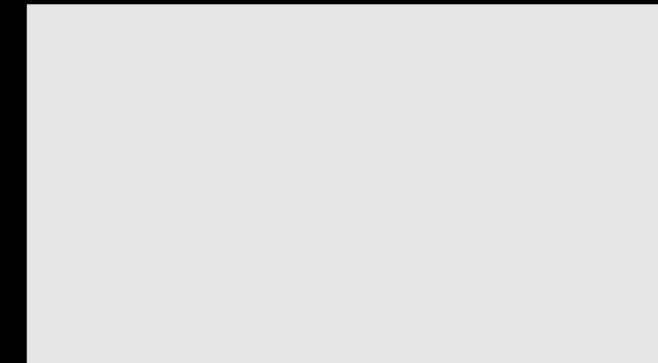
LPO validation station at IBTA plugfest 24



LPO/RTL validation at OFC'24



OIF-CEI interop demo at OFC'24 (dry run)



Keysight Mol for LPO testing



Keysight track record testing LPO



Keysight solutions for the industry

- ✓ AresONE 800GE Layer 1-3 traffic generation to stress test LPO performance
- ✓ Prototype of novel “EECQ” metric available on FlexDCA
- ✓ N1077B – 64Gbd SM & MM CDR
- ✓ M8050A BERT unmatched performance as “LPO”-compatible host (Tx and Rx)
 - Up to 20dB channel (de)-embedding with M8042A pattern generator
 - Advanced equalization capabilities and sensitivity of M8043A error detector

Keysight participation in industry standards

- ✓ OIF CEI-112G-Linear project
 - Technical contributions ([EECQ](#), [overview](#), [Tx test](#))
 - Partnering with industry (MACOM, Eoptolink, Innolight, etc.)



- ✓ LPO MSA member



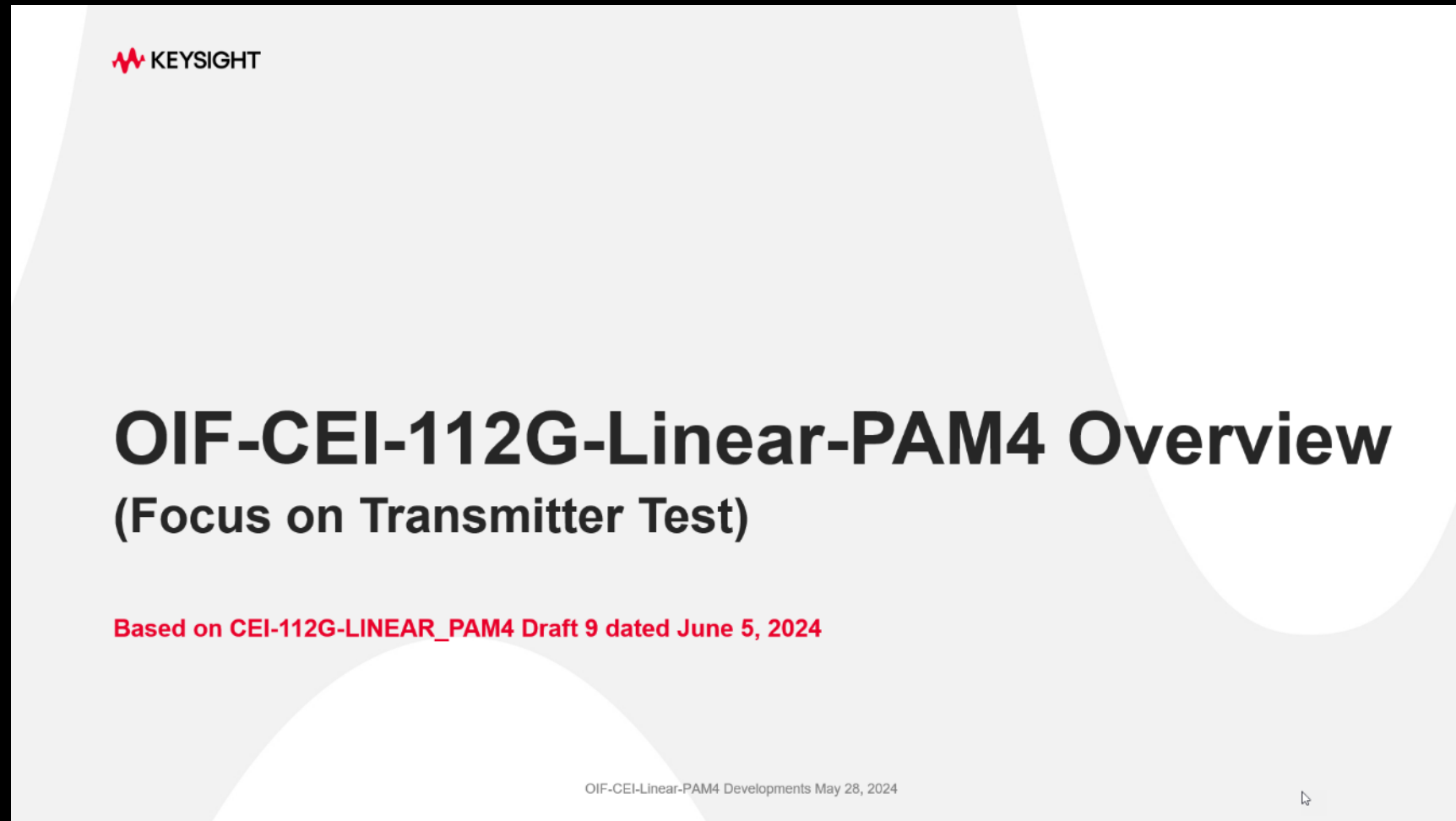
- ✓ LPO test dry run at InfiniBand Plugfest'24
- ✓ LPO interoperability at Ethernet Alliance plugfest'24 with 800GE AI switches



Public demo

- ✓ **World's first LPO interop demo @ ECOC'23 (OIF-CEI)**
- ✓ **interop demo @OIF-CEI booth @ OFC'24**
 - M8050A as LPO-compatible host Tx & Rx
 - N109x for TP2 optical measurements
 - N1060A for TP1a/TP4 electrical measurements
- ✓ **LPO functional test @ OFCC'24**
 - G800GE as LPO-compatible host Tx & Rx
 - N109x for TP2 optical measurements
 - N1060A for TP1a/TP4 electrical measurements

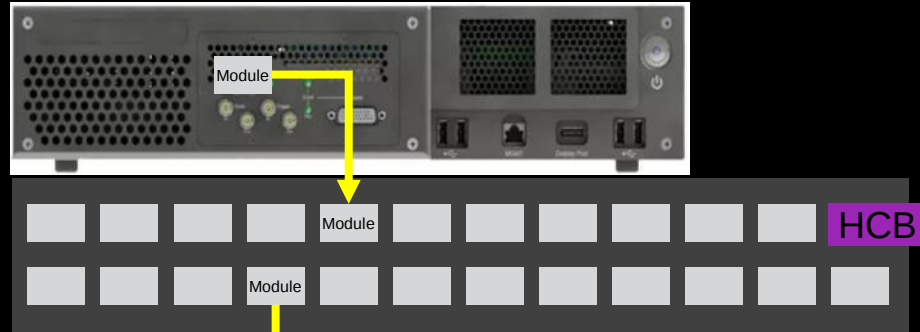
Keysight Method Of Implementation for LPO MSA and OIF-CEI Linear (Available on Request)



Keysight LDO demonstration

Keysight at OIF-CEI-Linear interop demo (ECOC'23)

G800GE Traffic Generator



Broadcom TH5 switch

N1092x DCA-M Oscilloscope with built-in CDR



TP2

N1000A DCA-X mainframe with N1060A "MegaModule"



TP1a

M8040A/M8050A Pattern Generator (PG)



EVB

Opt Tx

Module (DUT)

MCB

TP4

Keysight - Testing LPO Interfaces

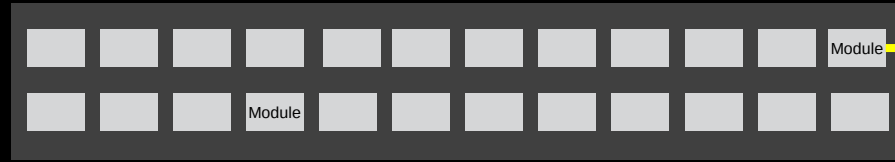
N1092x DCA-M Oscilloscope with built-in CDR



Keysight LDO demonstration

Keysight at OIF-CEI-Linear interop demo (OFC'24)

Broadcom TH5 switch



Multimode (VCSEL) LPO



N1092x DCA-M Oscilloscope
N1077B CDR



Keysight LDO demonstration

Keysight at OIF-CEI-Linear interop demo (OFC'24)



M8040A/M8050A Pattern Generator (PG)



Wilder
MCB

Opt Tx

LPO eval
board

TP4

N1092x DCA-M Oscilloscope
with built-in CDR TP1a



Keysight LDO demonstration

Keysight booth at OFC'24



Linear Drive Optics Test Demonstration



[click to view demo]



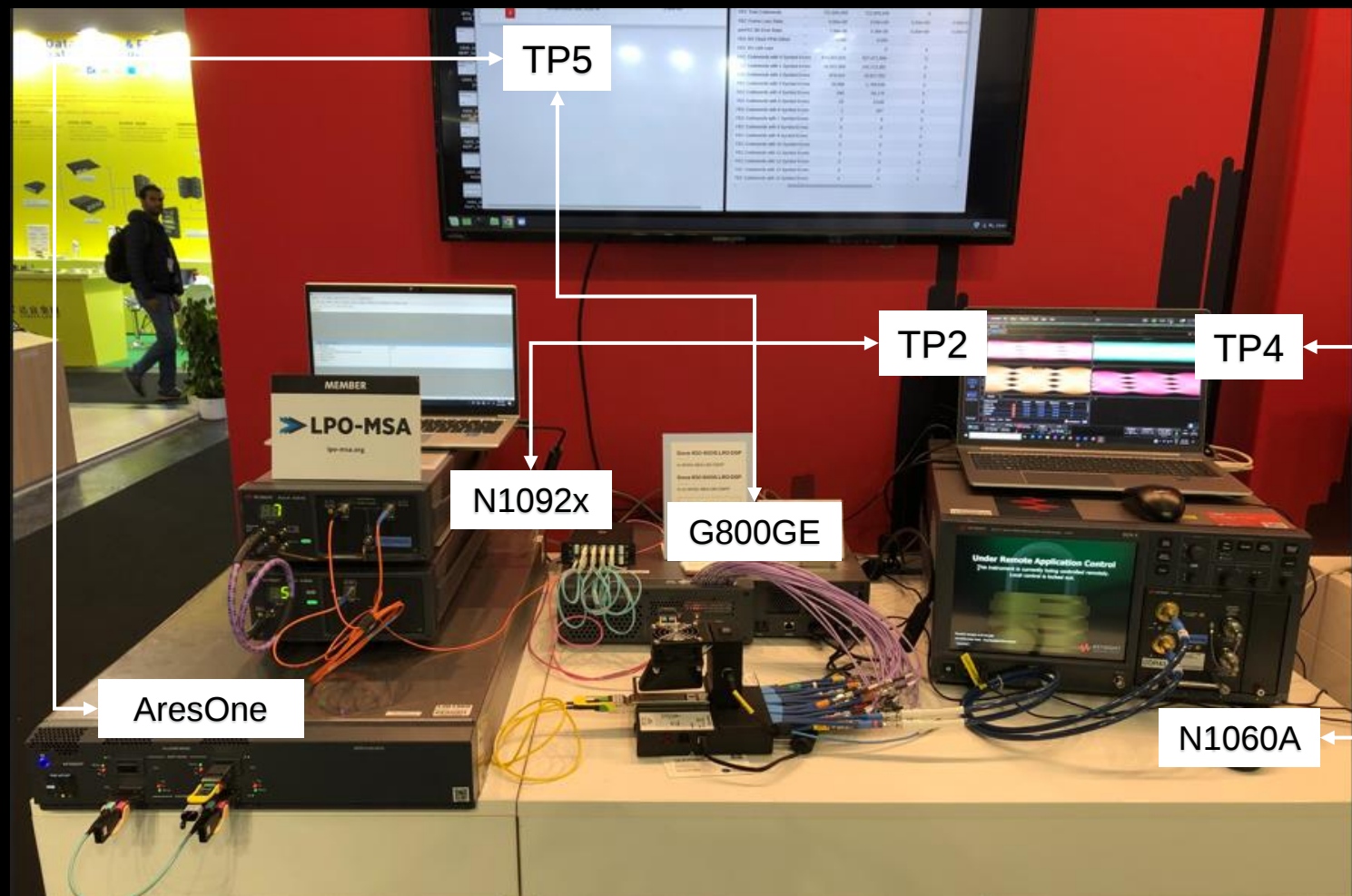
Keysight LDO demonstration

Keysight booth at ECOC'24

LPO vs RTL R Demonstration



[click to view demo]

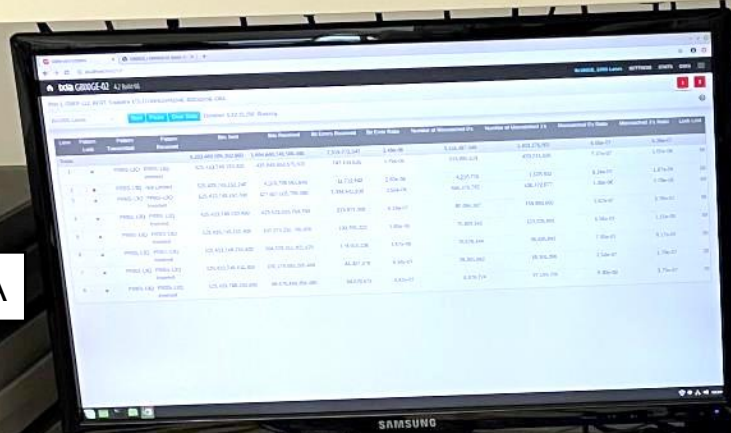


Power supply for MCB cooling fan (48V) set as +24 V and -24 V

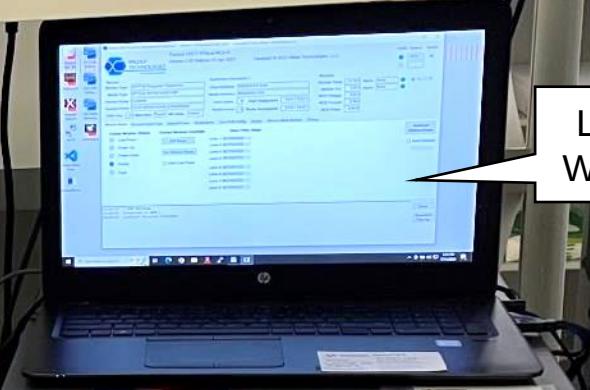
REMOTE DEMO SETUP
Please do not disturb.
Contact paul_forrest@keysight.com tel 577-3043

N1078A

N1092A



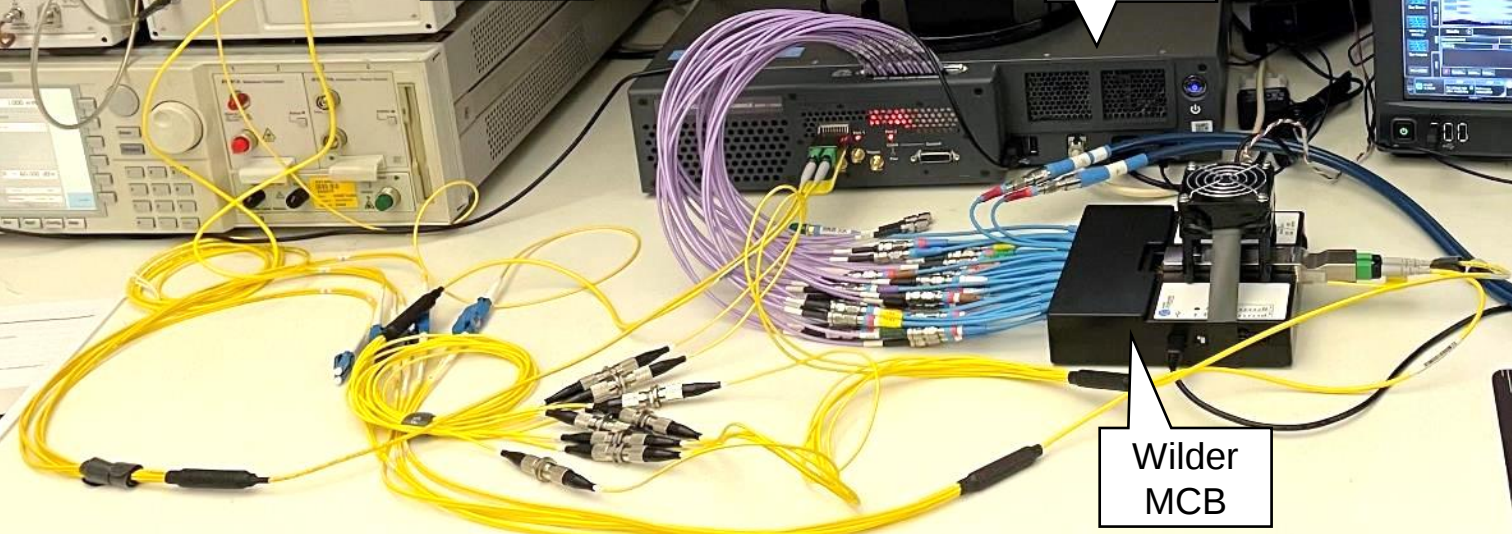
G800GE



Laptop running Wilder MCB GUI



DCA-X

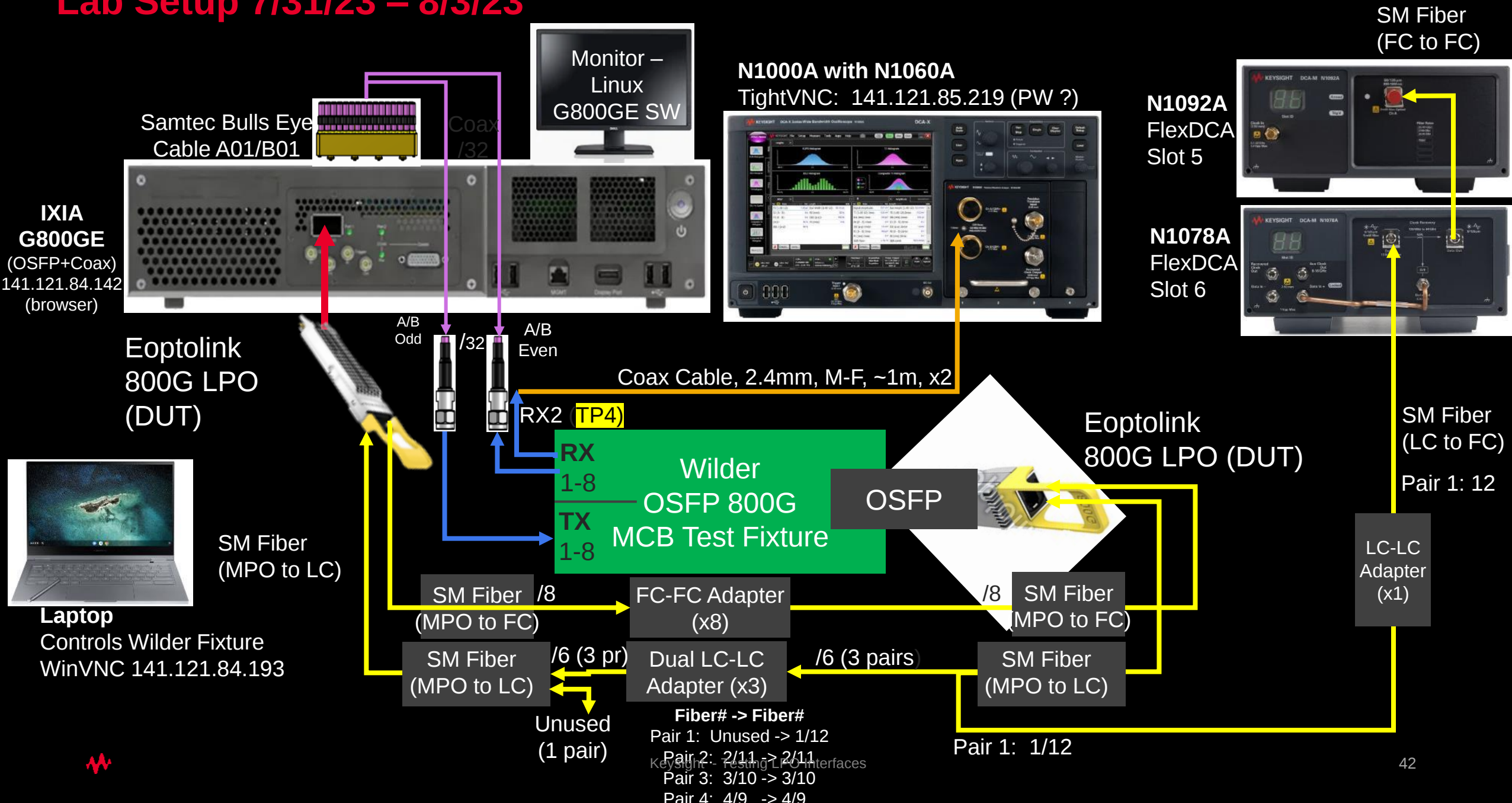


Wilder MCB



Mice: G800 MCB GUI DCA

Lab Setup 7/31/23 – 8/3/23



LPO validation setup (IBTA plugfest, April 24)

TP2 & TP4 measurements

Retimed module for
optical input test at TP3

TP2

TP4

DUT (LPO)

Host Tx
(M8050A PG)

TP3

TP0