

Compute Express Link® (CXL®) Protocol Analysis



Key Features

Find errors fast

- One button error check
- Fast upload speed
- Large trace memory
- Powerful triggering/filtering

See and understand the traffic

- Get useful information
- More choices of data views
- More ways to analyze data
- Custom decoding and reports

Data capture

- 100% data capture up to 64.0 GT/s

Supported platforms

CXL is offered as an optional feature on the following Teledyne LeCroy PCIe® protocol analyzers and/or exercisers:

- Summit M616 PCI Express Analyzer/Exerciser
- Summit T516 PCI Express Analyzer
- Summit Z516 PCI Express Exerciser
- Summit T54 PCI Express Analyzer
- Summit M5x PCI Express Analyzer/Jammer



Compute Express Link (CXL) is a new high-speed CPU-to-Device and CPU-to-Memory interconnect designed to accelerate next-generation data center performance. CXL is based on the PCI Express® Physical layer with speeds up to 64GT/s. CXL technology maintains memory coherency between the CPU memory space and memory on attached devices, which allows resource sharing for higher performance, reduced software stack complexity, and lower overall system cost. This technology enables system operations to focus on target workloads as opposed to the redundant memory management hardware in their accelerators.

Teledyne LeCroy protocol tools can exercise, emulate, capture, decode, monitor and verify all of the various operations on the CXL link. Firmware and driver developers can use this test equipment to support development, debug, verification and validation of both PCIe and CXL devices. The CXL standard defines three protocols that are dynamically multiplexed together: CXL.io, CXL.cache, and CXL.mem.

By showing the transported flit through the entire link and transaction layers on the flex bus, these protocol analyzers are versatile to support protocol analysis at all layers from the FlexBus Physical layer and Flits all the way up to the Link and Transaction Layers. Protocol analyzers

make use of the PCIe connectors for probing the DUT. These CXL protocol test solutions will provide the most useful decodes and various types of analysis and reports that help shorten development and testing time.

This trace shows a Link Layer Control Flit, and CXL.cache packets in a CXL Transaction. An error is indicated in Reserved field in the CXL.cache packet.

Packet 22	R→	32.0 x8	LLCTRL	Type	SubType	Full_Ack	Idle	Time Stamp				
			LLCRD	Ack	0x01	0x01	7.250 ns	0000 . 000 000 325 250 s				
3 CXL NULL flit Packets 24-28	R→	32.0 x8	NULL	Time Delta	Time Stamp							
				34.000 ns	0000 . 000 000 334 500 s							
Packet 32	R→	32.0 x8	NULL	Idle	Time Stamp							
				8.000 ns	0000 . 000 000 368 500 s							
Packet 34	R→	32.0 x8	Cache	H2D Response	OpCode	MESI	RSP_PRE	CQID	Idle	Time Stamp		
				GO	Error	Hit	0x002	0x002	7.750 ns	0000 . 000 000 376 500 s		
Packet 36	R→	32.0 x8	Packet Error	Cache	H2D Data Header	CQID	ChunkValid	Poison	GO_Err	Rsvd	Idle	Time Stamp
			RsvdErr			0x002	0	0	1	0x11	0.000 ns	0000 . 000 000 385 250 s
Packet 37	R→	32.0 x8	Cache/Mem	Data chunk	Data	Idle	Time Stamp					
					4 dwords	0.000 ns	0000 . 000 000 385 250 s					
Packet 38	R→	32.0 x8	Cache/Mem	Data chunk	Data	Idle	Time Stamp					
					4 dwords	6.000 ns	0000 . 000 000 385 250 s					

		Byte #0										
		7	6	5	4	3	2	1	0	7	6	5
Flit CXL.io	Protocol ID	0										
	1	Len 0x6				STP 0xF				FP 1		TC 0x0
	2	Fmt 0x2			Type 0x0				T9 0			
	3	RequesterId 0x7100										
	4											
	5											
	6											
7-16	Idle											
17	IO Reserved											

The Flit View from the CXL Trace shows a CXL.io Flit. Flits contain slots that carry one or more request/response messages or data chunks. The Flit header is also part of the slot.

The Flit View from the CXL Trace shows a CXL.cache/CXL.mem Flit. In this case, Flits contain slots that carry one or more request/response messages or data chunks.

		Byte #0										
		0	1	2	3	4	5	6	7	0	1	
Flit CXL.cache/CXL.mem	Protocol ID	0										
	Header	Type 0	Rsvd [1] 0	Alk 0	BE 0	Sz 0	Slot0 0x1			Slot1 0x0		
	Slot 0: H1	2-4										
	Slot 1: G0	5	Data 0xFF									
		6	Data 0xFF									
		7	Data 0xFF									
		8	Data 0xFF									
	Slot 2: G0	9-12										
	Slot 3: G1	13-16										
Flit CRC	17											

QuickTiming markers not set				
Traffic Summary Report				
Header Fields for packet #9, TLP Memory Write (32 bit) Flits for packet #9, TLP				
Go 0 of ### - Packet ###				
	Type	D2H/S2M (Upstream)	H2D/M2S (Downstream)	Total
	CXL Cache Request	71998	0	71998
	CXL Cache Response	0	41518	41518
	CXL Cache Data Header	6146	109448	115594
	CXL Mem Request	NA	0	0
	CXL Mem Request with Data	NA	0	0
	CXL Mem Response	0	NA	0
	CXL Mem No Data Response	0	NA	0
	CXL Cache/Mem Data Chunk	35100	215188	250288

Traffic Summary shows the CXL.io, CXL.cache and CXL.mem transactions upstream and downstream. Hyperlinked events bring you, with a single click, to the exact position in the trace where they occurred.

Ordering Information

Product Description

- Compute Express Link (CXL) Analysis option for Summit M616
- Compute Express Link (CXL) Exerciser/Generation option for Summit M616
- Compute Express Link (CXL) Analysis option for Summit T516
- Compute Express Link (CXL) Analysis option for Summit T54
- Compute Express Link (CXL) Analysis option for Summit M5x
- Compute Express Link (CXL) Exerciser/Generation option for Summit Z516
- CXL Compliance Test license for Summit Z516
- CXL Compliance Test license for Summit M616

Product Code

- PE6050SUA-A
- PE6070SUA-A
- PE550SUA-A
- PE391SUA-A
- PE392SUA-A
- PE370SUA-A
- PE376SUA-A
- PE6077SUA-A



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