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Time-Domain Techniques for De-embedding and Impedance Peeling

TECHNICAL BRIEF

Peter J. Pupalaikis
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Summary

This brief explains time-domain techniques for de-embedding that are available within the WavePulser 40iX called *time gating* and *impedance peeling*.

In addition, methods of using these time-domain techniques with coupled lines are explored.

Introduction

De-embedding is a common problem in making signal integrity measurements because often, the interconnection between the measurement instrument and the device under test (DUT) requires fixtures, cables, and/or probes. While usually it is not too much of a problem to calibrate the instrument to the end of the cables, which present a coaxial connector as the instrument port, the removal of what is between the instrument port and the desired reference plane of the DUT can prove problematic.

Many techniques are possible within the WavePulser 40iX for de-embedding such as calibration, and adapter and fixture de-embedding. These techniques are well known by engineers who are familiar with microwave measurements and the vector network analyzer (VNA).

Less well known are time-domain techniques that are available in the WavePulser. These techniques are related to *port extension* employed in the VNA. These time-domain techniques will be described subsequently.

Adapter De-embedding

Many de-embedding applications involve the assumption that there is a two-port device (adapter) connected between one or more ports of the measurement instrument and the ports of the DUT [1]. Figure 1 shows the de-embedding problem posed for a two-port measurement, where the problem is stated as:

> Given the known s-parameters of a system consisting of a left and right adapter connected to ports 1 and 2, respectively, each connected to the DUT, where the s-parameters of the adapters are known, what are the s-parameters of the DUT?

This problem has a relatively easy solution, but it requires information that is sometimes the most difficult to obtain – what are the s-parameters of the adapters? If the adapter is a coaxial device, like a bullet, this is easily obtained through measurement of the device. This paper concerns itself with de-embedding problems where one side of the adapter is not coaxial, for which a direct measurement of the s-parameters is difficult or impossible to obtain.

Time Gating

De-embedding is not a panacea. Usually, when connecting between instrument ports and the DUT, the desire is to have as transparent a connection as possible. This means a characteristic impedance as close to 50 Ω as

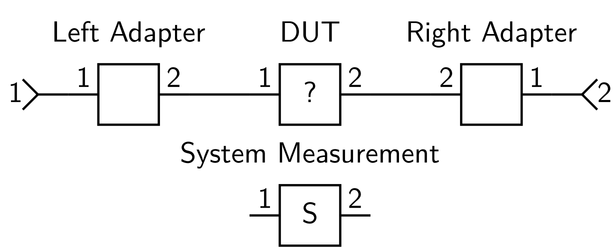


Figure 1: Adapter de-embedding

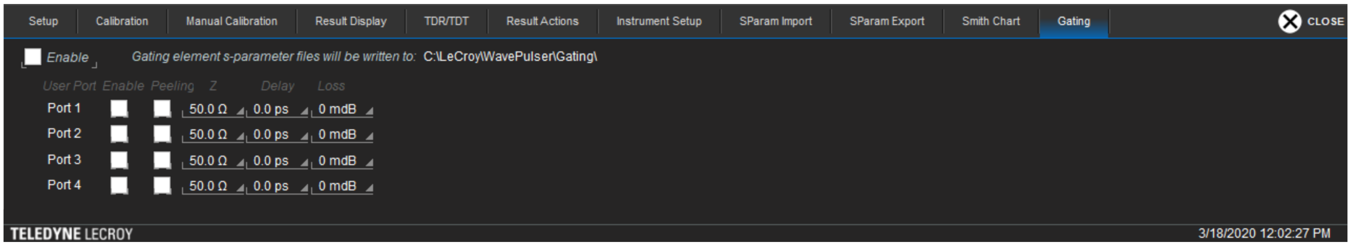


Figure 2: WavePulser 40iX time gating setup menu

possible, and as little loss as possible. Otherwise, even if the s-parameters of the intervening device are known, it degrades measurement performance, even when employing proper de-embedding algorithms.

Even if the quality of the connection is good, there's always the element of time. Even a well matched, low-loss adapter will have some amount of electrical length (i.e., it will take some amount of time for the waves to propagate through the adapter). In this situation, a very simple form of de-embedding, called *time gating*, can be used.

The gating setup menu is shown in figure 2. This menu is selected by clicking on a tab in the setup menu area of the display.

At the top of the menu is the global Enable check box, that enables or disables all gating operations. To the right is the folder where all gating s-parameter files will be written. This will be explained later.

Below that is a list of ports. This list will depend on the setting of the number of ports in the device being measured and whether they are single-ended or mixed-mode. For each port there is an Enable check box, followed by a Peeling check box, followed by characteristic impedance labeled Z, a Delay value and a Loss value.

In the simplest form of time gating, a 50 Ω section of transmission line with a specified electrical length is de-embedded from the DUT measurement. A user checks the global Enable checkbox to enable gating, checks the Enable checkbox for a given port, and enters the electrical length in the Delay box. If a measurement has already been completed, pressing the Recalculate button in the upper right of the WavePulser window causes the DUT s-parameters to be recalculated using the entered Delay value.

If there is any question about what gets de-embedded, one can recall the Touchstone file for the de-embedded device in `C:\LeCroy\WavePulser\Gating`. If it is known that the transmission line section is some other impedance than 50 Ω, then that value can be entered in the Z box. Finally, there is an option to enter a predetermined value in Loss. This value defines a linear loss in dB/GHz/ns.

Impedance Peeling

While time gating is a very simple form of de-embedding used mostly to account for time delay (or electrical length), an improvement can be made by measuring and accounting for the actual impedance of the line, even as the impedance changes over time. This can be performed automatically and is called *impedance peeling*. [2]

Figure 3 shows multiple lanes of measurement along with a 1× thru de-embedding structure. Plots of measurements of the 1× thru structure are provided in figure 4. This structure is a calibration element built onto a test fixture and is intended to be representative of the traces from an SMA connector to the DUT on a fixture. The idea here is that the user measures this trace, and then de-embeds this measurement from measurements of the DUT. Note in figure 3 that the 1× thru structure has an SMA connector on each end while the trace structure for the DUT measurement has only one. In this situation, one would ideally de-embed at least one of the SMAs from the 1× thru. In this example, in order to illustrate impedance peeling, we will de-embed both SMAs in an effort to determine the actual 1× thru trace in between them.

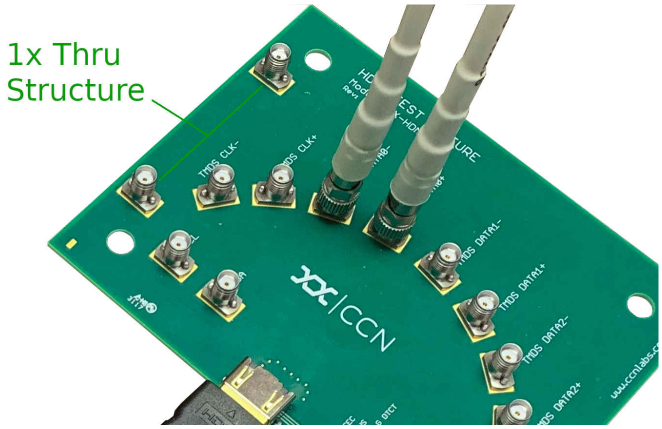


Figure 3: Fixture with 1× thru de-embedding structure (used with permission from CCN, `www.ccnlabs.com`)

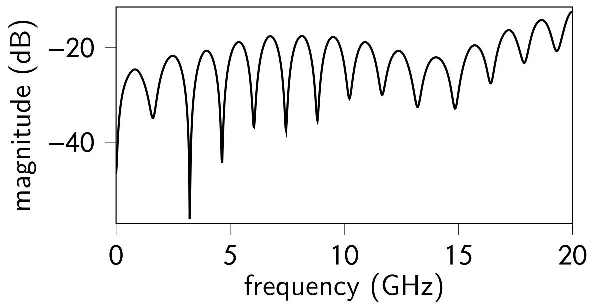
The magnitude and phase of the return loss (s_{11}) measurement of the entire trace is shown in figures 4a and 4b, which don't show anything useful except that the trace is somewhat non-ideal. The magnitude and unwrapped phase of the insertion loss (s_{21}) measurement is shown in figures 4e and 4f, which show that the trace has an electrical length of 443 ps and has a linear loss characteristic providing 6 dB of loss at 20 GHz.

It is always important to examine the time-domain performance of s-parameters used for signal integrity. The impulse and step response corresponding to the s_{21} are shown in figures 4g and 4h, which show the time-domain effect of the loss in the trace. Most important, for impedance peeling purposes, the s_{11} impulse and impedance plots are shown in figures 4c and 4d. In figure 4c, one can observe that the impedance bounces around between 51 and 48 Ω for the first few points and then jumps to approximately 53 Ω until about 400 ps when the connector on port 2 is encountered. Because the s-parameters provided are 800(+1) points from DC to 20 GHz, the effective sample rate in the time domain is 40 GS/s and the sample period is 25 ps. Because each sample of the impedance profile is for a wave that has propagated down and back from an interface, the sample period for the impedance plot in figure 4d is 12.5 ps per point. There are four impedance points for the connector accounting for $4 \cdot 12.5 = 50$ ps of electrical length.

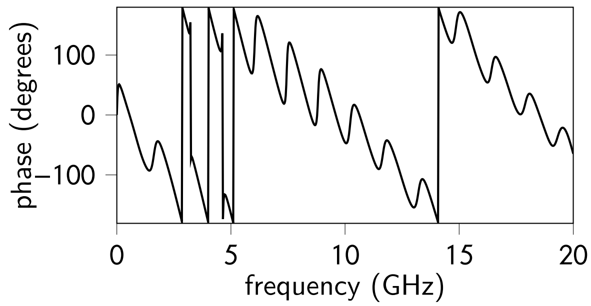
An example of the internal structure of an impedance peeling de-embedding situation is shown in figure 5. Here, a model is provided for the connector at port 1 in figure 5a and at port 2 in figure 5b. These models were created by assembling a cascade of transmission line sections, each lossless and having electrical length of 12.5 ps. The models for the connectors are de-embedded in figure 5c. This is the same situation as *adapter* de-embedding (see [1]), but instead of providing the s-parameters of the adapter, the instrument determines the model for the adapter automatically from the impedance profile.

As mentioned previously, the WavePulser provides the s-parameter measurements of the peeled structures in a directory stated on the user interface. These s-parameters can be recalled by the user and examined for any reason. Plots of these s-parameter files are shown in figure 7 and figure 8. The s_{11} and s_{21} frequency-domain responses for the models of the connectors are shown for port 1 in figures 7a, 7b, 7e, and 7f, and for port 2 in figures 8a, 8b, 8e, and 8f, where they are not seen to have a very large effect, which is why time gating is often used. This is also seen when examining the s_{21} impulse and step responses for port 1 in figures 7g and 7h and for port 2 in figures 8g and 8h. The effect of these connectors is mostly to provide 50 ps of delay.

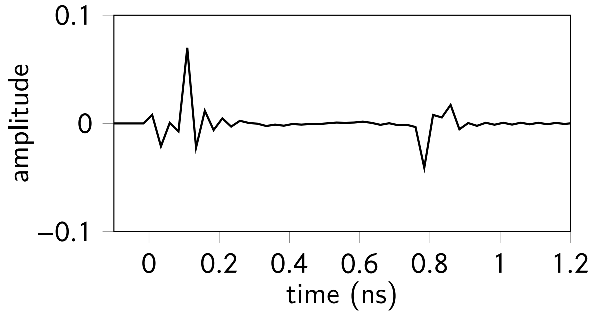
While it is unclear whether there is loss in the connector (here, the choice is to assume they are lossless), one can apply the loss of the measured trace over the connectors, as well. Here, based on the magnitude response shown in figure 4e, a reasonable choice would be 6 dB/20 GHz/0.442 ns = 667.5 mdB/GHz/ns. This would have each connector providing $0.6675 \cdot 0.05 \cdot 20 = 667.5$ mdB at 20 GHz. The user would have to decide this for themselves, either from knowledge or simulation of the connector or by other means.



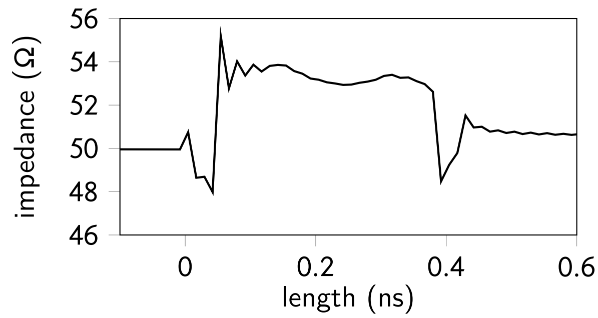
(a) Magnitude



(b) Phase

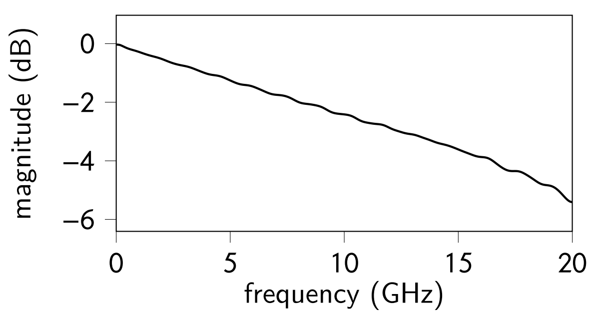


(c) Impulse response

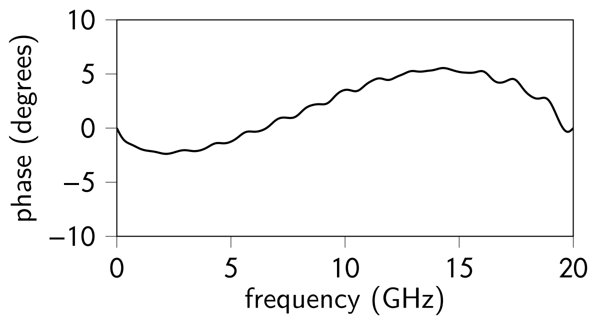


(d) Impedance profile

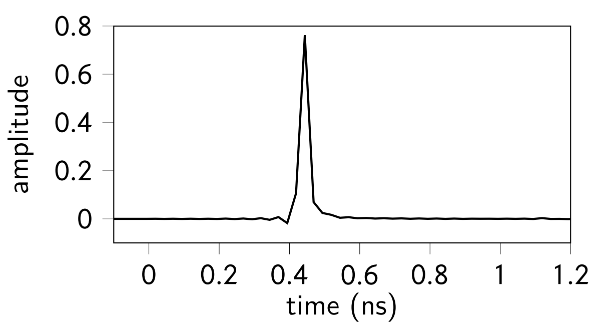
s_{11}



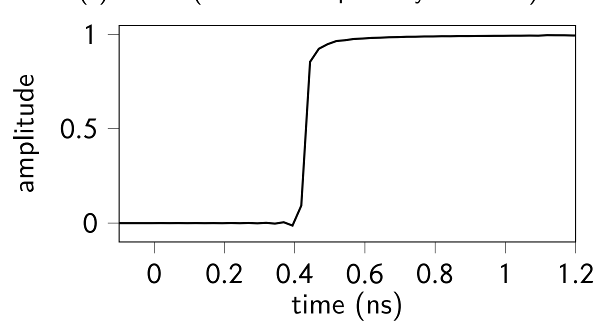
(e) Magnitude



(f) Phase (with 442.74 ps delay removed)



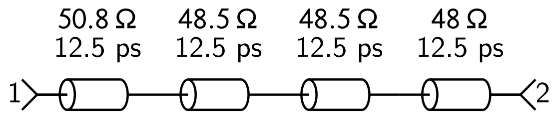
(g) Impulse response



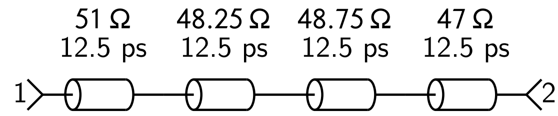
(h) Step response

s_{21}

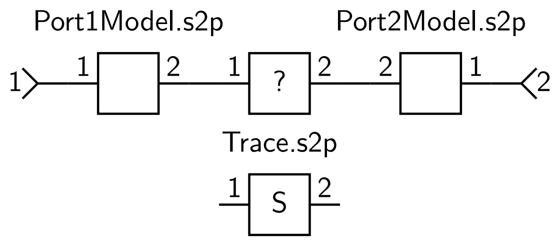
Figure 4: De-embedding trace structure



(a) Port 1 model



(b) Port 2 model



(c) Port 1 and 2 de-embedding

Figure 5: Impedance peeling de-embedding

To understand impedance peeling, the most important thing to see is the similarity between the impedance profile of the port 1 connector shown in figure 7d to the first 50 ps of the impedance profile of the trace shown in figure 4d. They are the same as expected, which makes the impedance peeling de-embedding method a reasonable de-embedding choice for small structures. Also important is the fact that the impedance profile for port 1 shown in figure 7d differs from figure 8d, making the s-parameters of the two connectors slightly different. Impedance peeling de-embedding measures each of the port impedances during de-embedding, allowing the de-embedding to dynamically adapt to different structures with only estimates of the length and loss provided.

Examination of Causality and Causality Enforcement

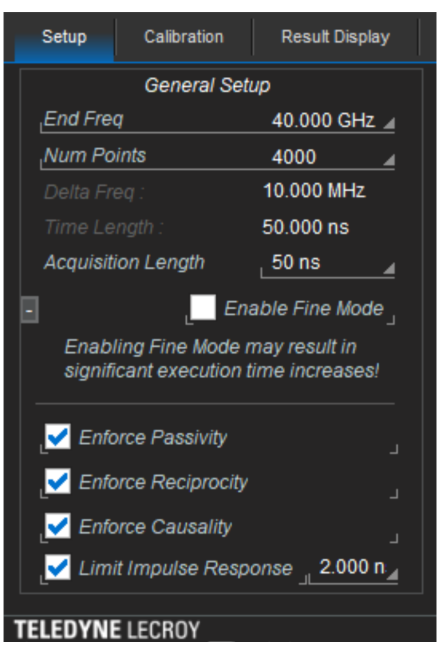


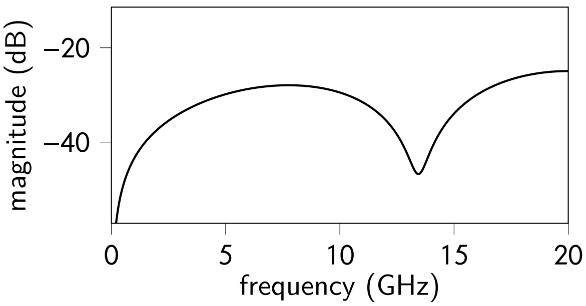
Figure 6: WavePulser 40iX setup

When performing any de-embedding, it's a good idea to examine and enforce causality on the result. Causality violations are when effects occur prior to zero time. These are best viewed and are most obvious in the time domain.

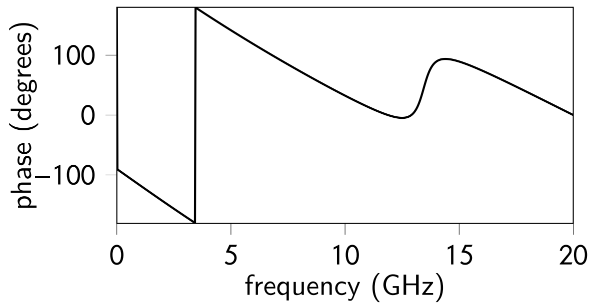
In figure 9, the impedance profiles shown are shown using various impedance peeling and gating methods. The variations shown involve peeling or gating, loss applied or lossless, and causality enforced or not. All of the results without causality enforcement shown in figures 9a, 9b, 9c, and 9d, show causality violations. Whether loss is applied or not seems to be irrelevant.

In figures 9a and 9b, time gating is seen to simply move the portion of the impedance profile of the connector prior to time zero. This is expected when de-embedding a 50 Ω section of line. As mentioned previously, if the line is essentially a perfect 50 Ω match, then this works well. Here, the causality violations are not that bad.

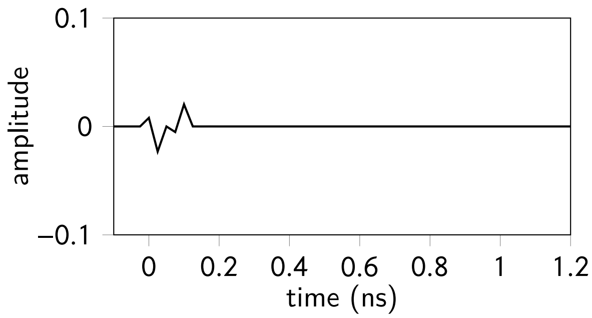
In the impedance peeling results shown in figures 9c and 9d, causality violations are still present, but they are smaller (actually very small). Again, the application of loss does not seem to affect the result. Causality violations are evidence of imperfect de-embedding. The obvious reason for lack of perfect results is that the structure being de-embedded does not match the actual structure, and this is the case here to a slight degree.



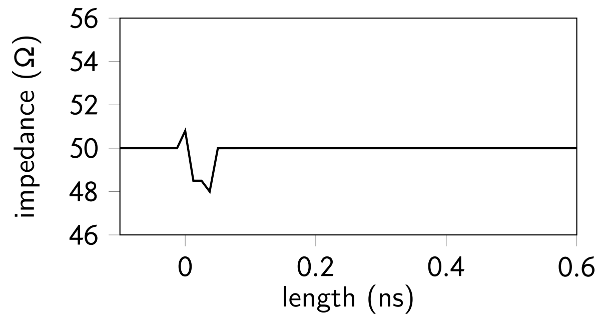
(a) Magnitude



(b) Phase

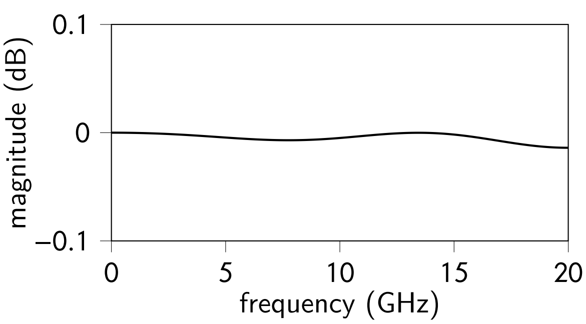


(c) Impulse response

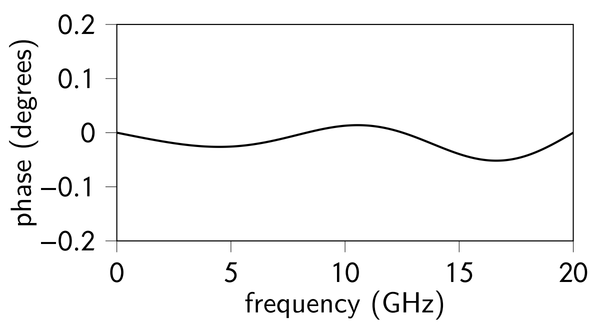


(d) Impedance profile

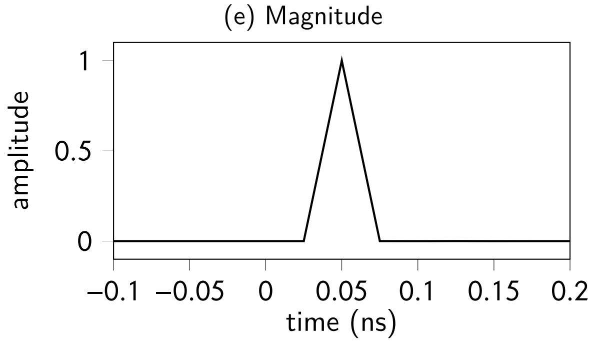
s_{11}



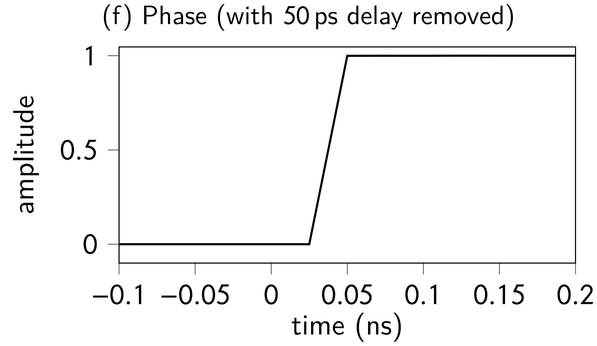
(e) Magnitude



(f) Phase (with 50 ps delay removed)



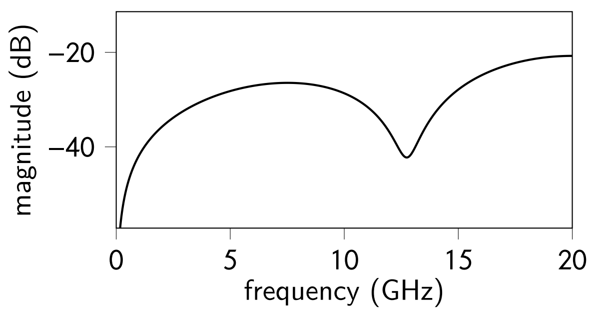
(g) Impulse response



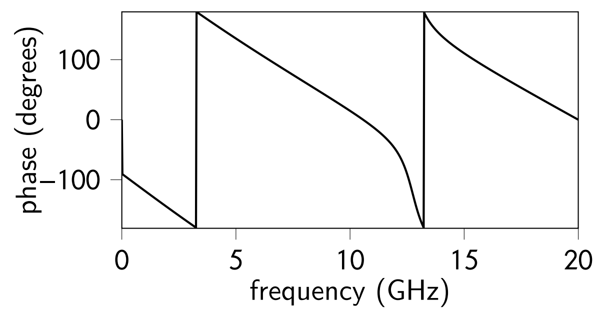
(h) Step response

s_{21}

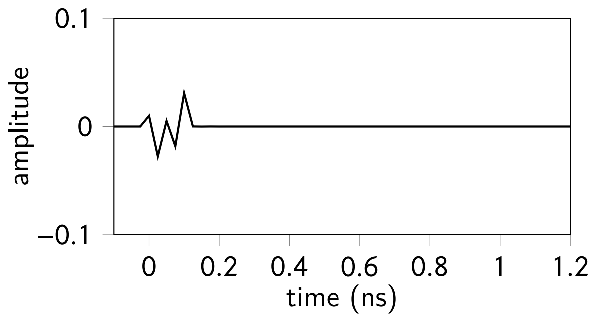
Figure 7: Port 1 de-embedding trace structure



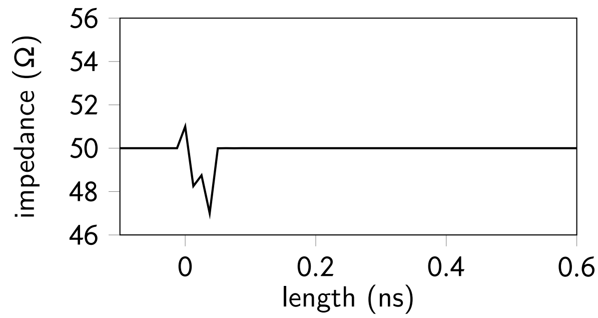
(a) Magnitude



(b) Phase

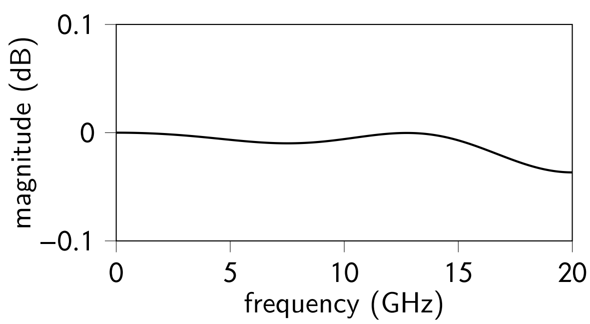


(c) Impulse response

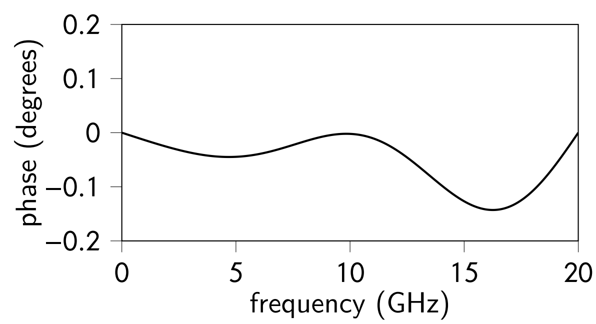


(d) Impedance profile

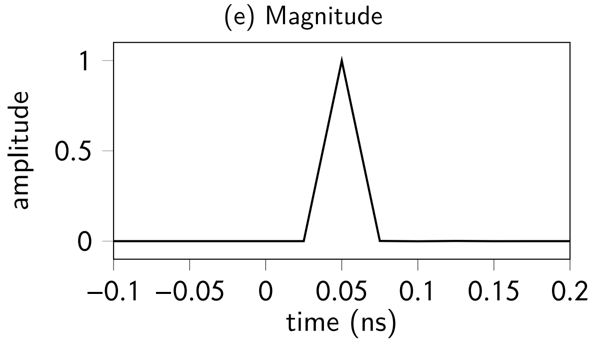
s_{11}



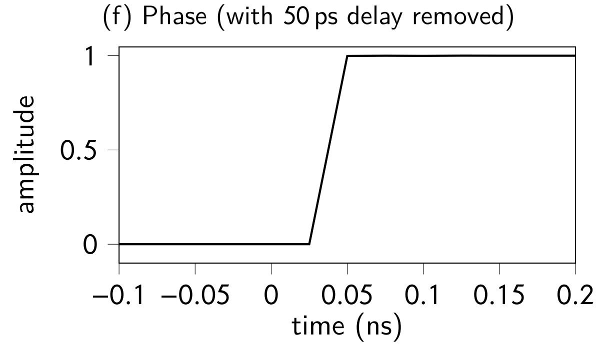
(e) Magnitude



(f) Phase (with 50 ps delay removed)



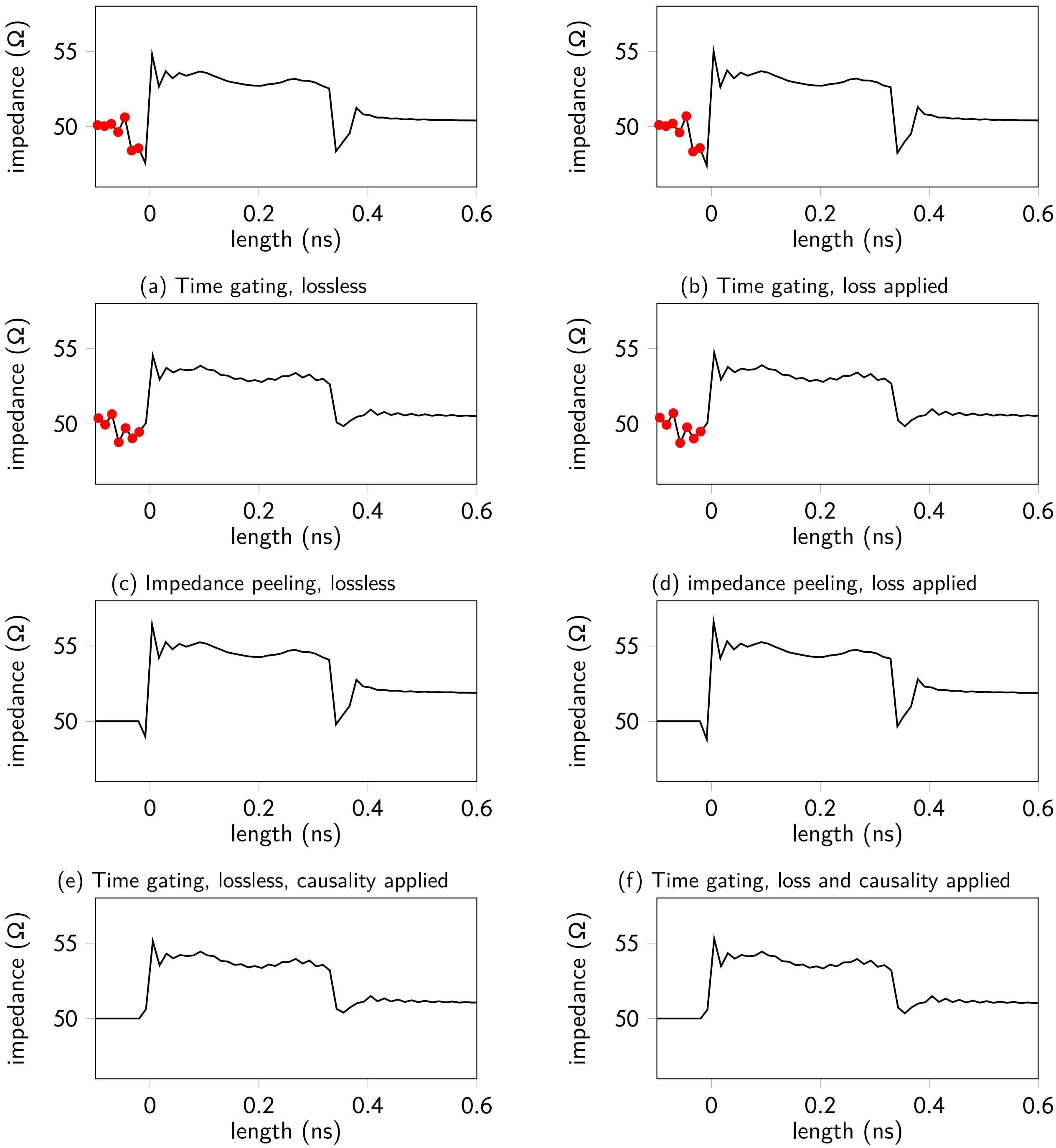
(g) Impulse response



(h) Step response

s_{21}

Figure 8: Port 2 de-embedding trace structure



(a) Time gating, lossless

(b) Time gating, loss applied

(c) Impedance peeling, lossless

(d) impedance peeling, loss applied

(e) Time gating, lossless, causality applied

(f) Time gating, loss and causality applied

(g) Impedance peeling, lossless, causality applied

(h) impedance peeling, loss and causality applied

Figure 9: Resulting impedance profiles under various peeling and gating conditions

The reasons could be that the loss is apportioned improperly among the sections in the model in figure 5a (it is lossless in figure 9c and the loss is evenly apportioned in figure 9d), but the most probable reason in this case is that the impedance discontinuity at the beginning of the connector shown as excess inductance followed by excess capacitance[1] might be formed by lumped inductance and capacitance. This can occur as the pin of the connector transitions into the board, and by any stubs formed. In any case, the imperfection using the peeling method is on the order of ±1 Ω.

After time gating and impedance peeling, or any de-embedding, it is advisable to enforce causality (see figure 6) on the results. Causality enforced results are shown in figures 9e, 9f, 9g, and 9h. Although this cleans up the time gating measurements, it is interesting to look at the back end of the impedance plots around 400 ps in figures 9e and 9f, where the impedance discontinuity of the port 2 connector remains. Because of the time gating, examination of the s_{21} step response shows that the signal takes 342.74 ps to propagate to the end, but this discontinuity appears later in the impedance profile. This is unavoidable when using time gating. When examining this same effect for the impedance peeling situation, one sees that this effect is negligible in figures 9g and 9h.

If the effect of the de-embedding on the opposite connector is objectionable, there is one more trick that can be employed that is somewhat heavy-handed, which is to limit the impulse response length whose control is shown in figure 6. In this example, since the trace ends at approximately 350 ps, the impulse response length can be limited to 700 ps, taking into account that the incident wave must go down the line and back again to form the impedance profile plot.[2]

Table 1: Fitted model parameters

Parameter	Value
resistance	113.9 mΩ
inductance	18.45 nH
conductance	95.8 μS
capacitance	6.37 pF
skin-effect resistance	39.5 $\mu\Omega/\sqrt{\text{Hz}}$
loss tangent	0.0228

The object of this exercise was to determine the de-embedding trace structure without the SMA connectors. Therefore, the final measurement with the connectors de-embedded through impedance peeling, causality enforced, and impulse response limited is used to fit a model of the line using the open-source *SignalIntegrity* software (see [4]). The parametric results of the fit are shown in table 1. The comparison between the model and the measurement is shown in figure 10, showing good agreement.

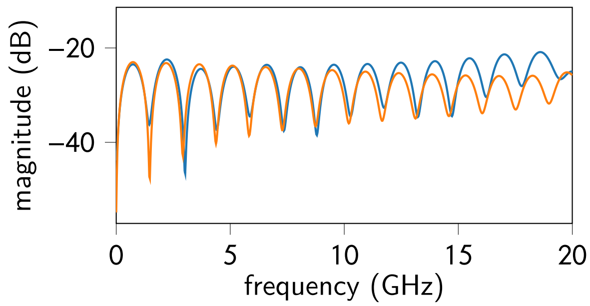
Impedance Peeling and Coupled Lines

As with any usage of the impedance profile, either for de-embedding or analysis, there is an assumption of lack of coupling. Coupling implies that the waves split off, propagating down different branches of the circuit. Certainly there can be no intelligent analysis of waves propagating back and forth in different branches when the impedance profile assumes a model of successive, linearly arranged, transmission line sections. This being said, there are ways to deal with coupled lines using these techniques. The answer is *mixed-mode* conversion. A mixed-mode s-parameter measurement setup within the WavePulser 40iX is shown in figure 11.

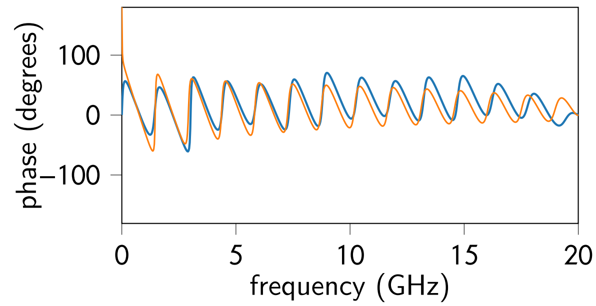
This paper will not go into detail on mixed-mode s-parameters, but consider that a transformation can be made of single-ended waves into modes that propagate with no interaction. This is the case when a differential transmission line, although coupled, is completely balanced, meaning each leg of the differential pair of lines is identical. In a balanced configuration, using mixed-mode converters, the differential transmission line can be thought to transmit the differential- and common-mode waves with no interactions between the modes. This means that it is possible to develop a differential-mode impedance profile as well as a common-mode impedance

[1] Impedance profiles show the balance between inductance and capacitance forming the characteristic impedance of the line as $Z_c = \sqrt{L/C}$, so an impedance rise can be viewed as excess inductance and an impedance dip can be viewed as excess capacitance.

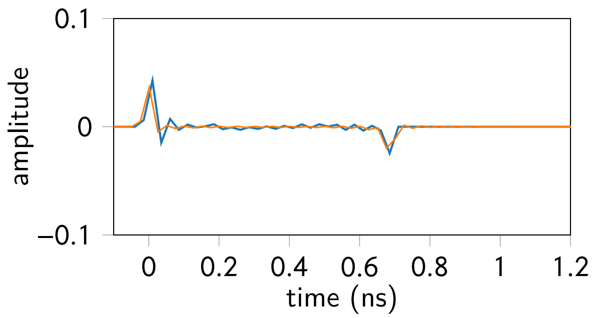
[2] Ideally, the s_{11} would want to be limited in impulse response length to 700 ps, but the s_{21} would want to be limited to 1.05 ns, to allow the thru response to propagate three times through the structure. See [3] for more details.



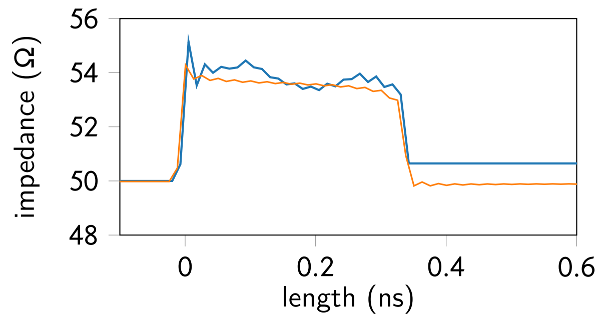
(a) Magnitude



(b) Phase (unwrapped)

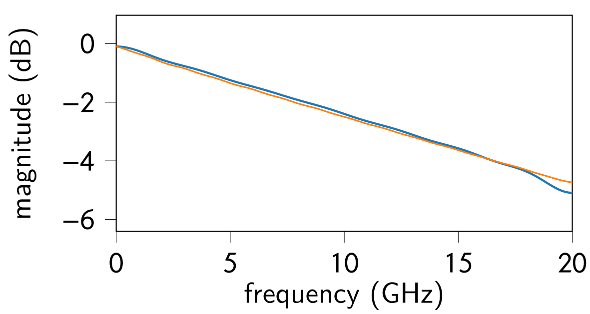


(c) Impulse response

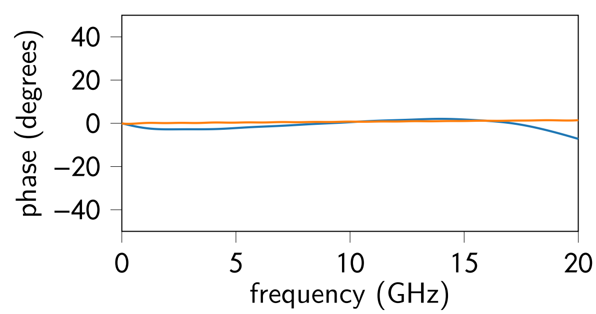


(d) Impedance profile

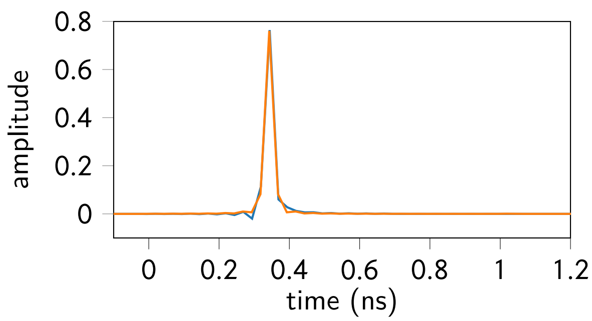
s_{11}



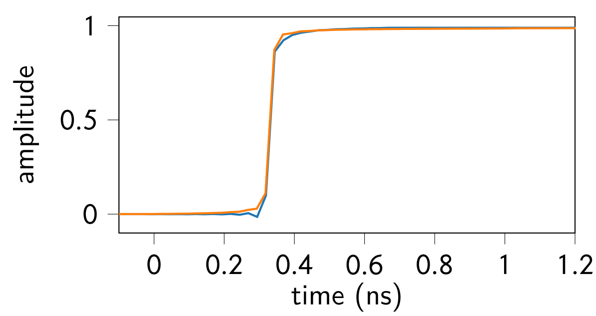
(e) Magnitude



(f) Phase (with 343 ps delay removed)



(g) Impulse response



(h) Step response

s_{21}

Figure 10: De-embedded trace with trace model (measurement is in blue, model is in yellow)

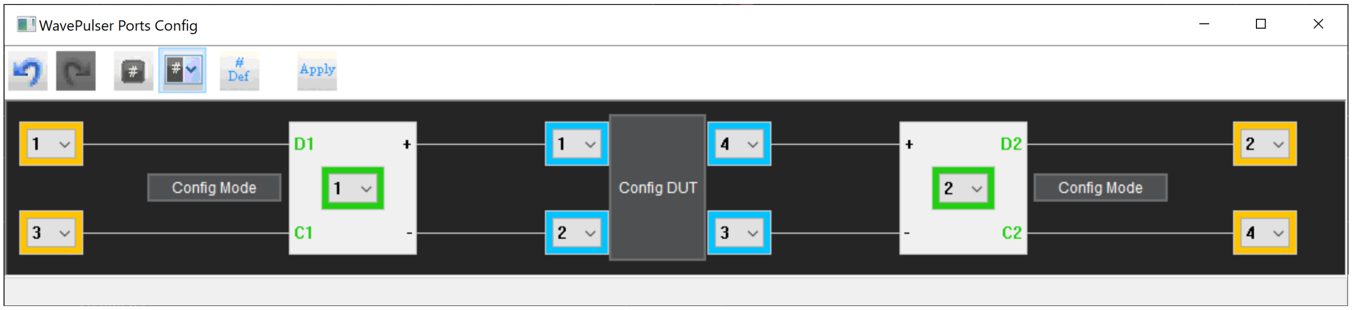


Figure 11: WavePulser 40iX mixed-mode conversion setup

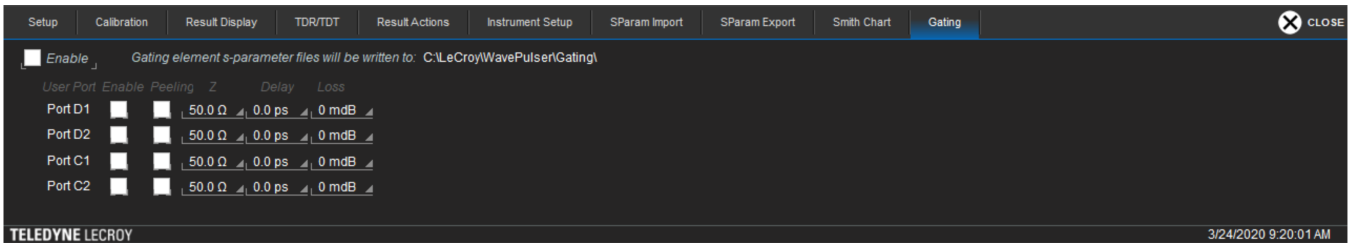


Figure 12: WavePulser 40iX time gating setup menu with mixed-mode measurements

profile, and if this is possible, impedance peeling and gating techniques are possible. Therefore, when measuring mixed-mode s-parameters, the Gating menu shows the mixed-mode ports for gating, as shown in figure 12. Note that when using gating or impedance peeling for de-embedding with mixed-mode s-parameters, the times for the differential and common modes will tend to be different, due to the different propagation velocities of the different modes. This should be checked by examining the impedance profile prior to performing the final de-embedding step.

Conclusion

Time-gating and especially impedance peeling has been seen to be useful de-embedding techniques that are easily performed with the WavePulser 40iX. A useful aspect of this technique is its use of the impedance profile measured directly at the time of the DUT measurement. Causality and impulse response time limiting have been shown to be effective in resolving any small errors created by de-embedding.

References

[1] P. J. Pupalaikis, "De-embedding with the WavePulser 40iX," Teledyne LeCroy Technical Brief, Mar. 2020.

[2] P. J. Pupalaikis, *S-Parameters for Signal Integrity*. Cambridge: Cambridge University Press, pp. 440-456, 2020.

[3] P. J. Pupalaikis, "WavePulser 40iX Pulser Repetition Rate and Frequency Resolution," Teledyne LeCroy Technical Brief, Mar. 2020.

[4] The *SignalIntegrity* project, `https://pypi.org/project/SignalIntegrity/` and `https://github.com/TeledyneLeCroy/SignalIntegrity/`.