APPLICATION NOTE

Conformance Testing of 800G Ethernet Links for the Data Center

100G / Lane test solutions

KEYSIGHT

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Introduction

With ever increasing bandwidth needs for video conferencing, streaming, digital entertainment, 5G, autonomous vehicles, trading, IoT etc., both electrical and optical links in the Data Center continue to move upward in throughput and data rate.

Current projects from the Institute of Electrical and Electronics Engineers (IEEE) and the Optical Internetworking Forum (OIF) standards associations are addressing the next generation in speed – 800G or 100G / lane.

This application note will cover the changes in requirements between 400G and 800G electrical interfaces and how Keysight Technologies Transmitter and Receiver Conformance Test Solutions allow users to easily perform design validation testing and explore their design margins.

New Standards

The move from 100G to 400G links was a revolutionary change going from NRZ (1 bit / symbol) to PAM4 (2 bits / symbol) signaling, bringing with it a number of new issues and consequently new measurements such as PAM4 linearity, signal to noise and distortion ratio (SNDR) and new test methods for eye height, eye width, VEC (vertical eye closure) etc.

The latest evolution to 800G may not seem that significant, since there are already 400G optical transceiver links running at 100G / wavelength (53 Gbaud PAM4), such as400GBASE-DR4 and 400G-FR4. However, the electrical lanes for these and all other 200 and 400G standards to date have operated at 50G / lane utilizing 8 x lanes at 26 Gbaud PAM4 per lane, like 400GAUI-8.

Current developments from the IEEE and OIF standards associations are addressing the next generation 800G Ethernet. Projects such as IEEE 802.3ck and OIF-CEI 112G specify the electrical link parameters and test methods for 53 Gbaud PAM4 and 38-58 Gbaud PAM4 respectively, based on 8 x PAM4 lanes, bringing 100G / lane to the electrical interfaces such as chip-to-module, chip-to-chip, backplane and copper cable.

Standards

The IEEE 802.3 Ethernet Working Group’s current project in this area is IEEE 802.3ck. This covers chip-to-chip (C2C Annex 120F), chip-to-module (C2M Annex 120G), copper cable (CR Clause 162) and backplane (KR Clause 163) interfaces.

The Optical Internetworking Forum Physical and Link Layer Working Group current projects are suite of Common Electrical Interface (CEI-112G) standards covering ultra-short (MCM), extra short (XSR), very short (VSR), medium (MR) and long reach (LR).

Although IEEE and OIF standards are highly leveraged from each other, there are some differences in parameter definitions and measurement methodology. Also, as baud rates increase so do losses in the transmission channel, leading to smaller and more distorted PAM4 signals. This necessitates changes to parameter definitions and test methods even from the previous 400G (50G / lane) standards.

OIF CEI-112G-VSR, -MR and -LR have an equivalent clause in IEEE 802.3ck as shown in table 1.

Table 1. OIF-CEI-112G and IEEE 802.3ck equivalent clauses

OIF-CEI Standard	IEEE 802.3ck Standard	Max. channel loss
CEI-112G-MCM	-	6 dB
CEI-112G-XSR	-	10 dB
CEI-112G-VSR	100GAUI-1 C2M[1]	16 dB
CEI-112G-MR	100GAUI-1 C2C[1]	20 dB
CEI-112G-LR	100GBASE-KR1[1]	28-30 dB
-	100GBASE-CR1[1]	24 dB

It generally takes a few years for a standard to progress from conception to being finalized and released. The physical layer aspects are usually complete well before the standards are final and it is essential for early adopters and test solution providers to be closely involved in the creation of these standards to ensure that the key parameters and test methods developed are both achievable and repeatable.

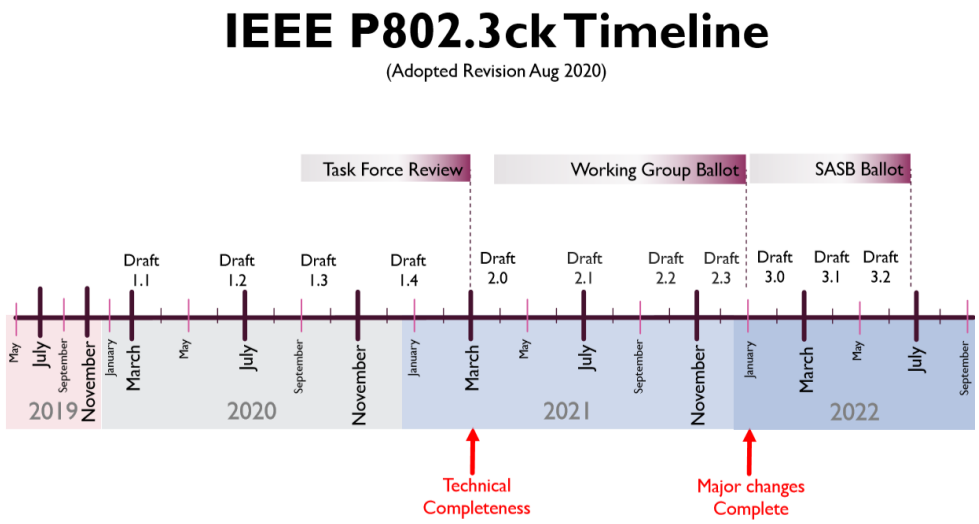

Figure 1. Life cycle of an IEEE standard [2]

[1] Also includes the 200GAUI-2, 400GAUI-4 and 200GBASE, 400GBASE variants
[2] IEEE 802.3 timeline

800G Design Cycle

Keysight Technologies is uniquely positioned to offer test and measurement solutions throughout the entire design cycle, from simulation, design validation, conformance test, protocol test and manufacturing. With close association and participation in the standards organizations, Keysight is able to provide first-to-market Conformance Test Solutions that can be updated as changes occur during the standards creation, allowing timely characterization and validation of component and systems designs to run concurrently with the standards development cycle.

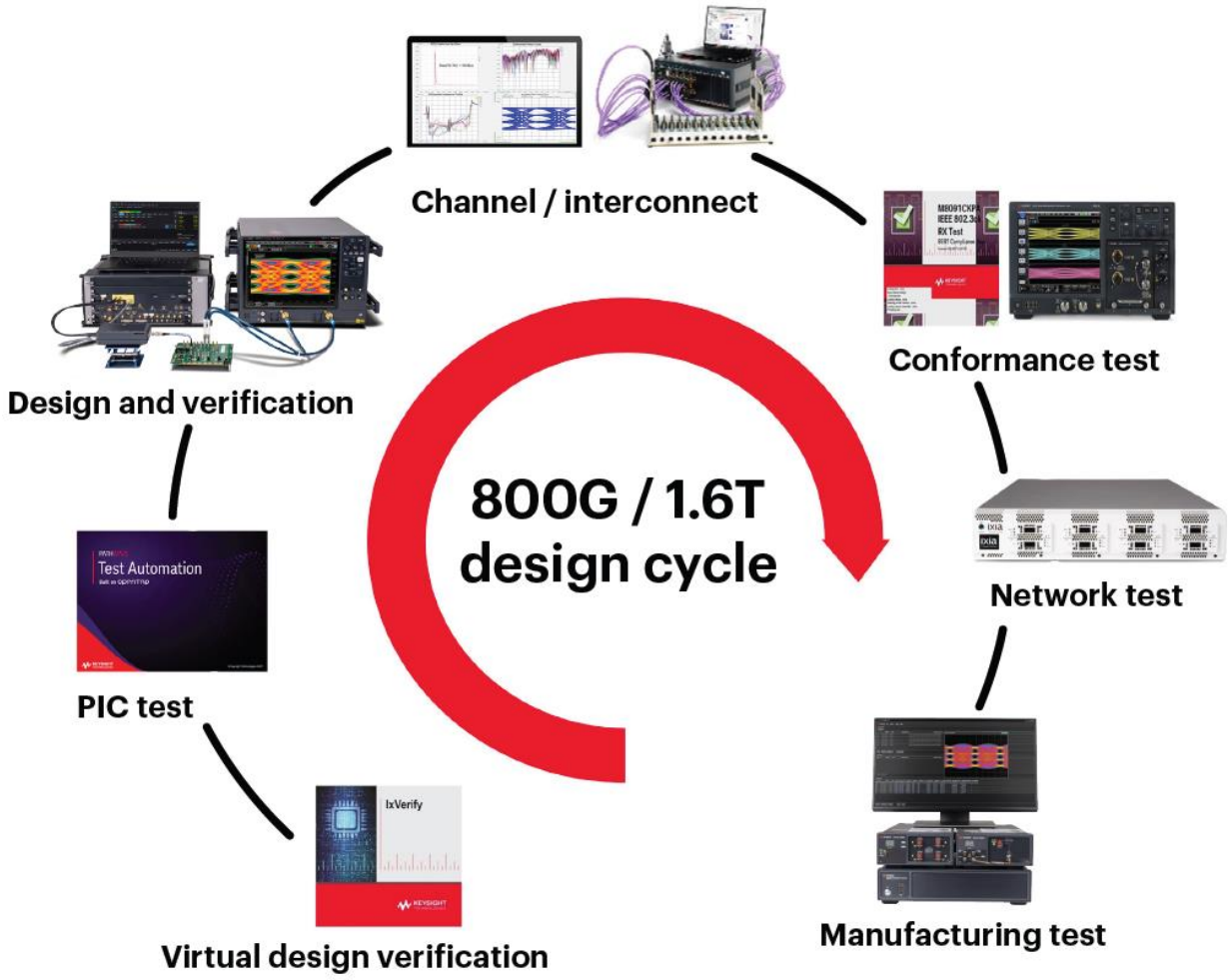

Figure 2. 800G Design Cycle

Changes in Requirements from 400G to 800G

With the increase in baud rate from 26 to 53 Gbaud come new challenges. The channel losses are higher and therefore require a higher degree of equalization to recover the signal at the receive end of the link. Tighter design margins and reflections in the channel necessitate more complex measurements at the 53 Gbaud rate which results in a longer and more intricate design and validation process.

For example, the IEEE802.3ck project has defined a new model for the reference receiver in the chip-to-module (C2M) interface which includes receiver input referred noise; a 3-pole 2-gain stage CTLE (Continuous Time Linear Equalizer) and 4-tap DFE (Decision Feedback Equalizer) with taps optimized using pulse response. Another change here is the use of a 4th order Butterworth filter as a noise filter (instead of the traditional 4th order Bessel-Thompson filter) for the eye width, eye height and vertical eye closure measurements. Test instrumentation noise needs to be accounted for when performing these measurements.

Chip-to-module measurements such as SNDR, VEC, eye height, eye width, even-odd jitter (EOJ) are still in use but there are substantial changes to the test methods for EOJ and VEC to improve correlation with real device and link performance.

Chip-to-chip, backplane, and copper cable conformance test is principally the same as previous standards with heavy reliance on channel operation margin (COM) methodology.

CTLE + DFE equalization is also required for the chip-chip, backplane, and copper cable links. On the transmitter side, 5-tap de-emphasis equalization is now mandatory for all interfaces with three pre-cursors and one post cursor. For conformance testing both transmitter and receiver equalization should be enabled to qualify the link performance. Finding the optimum combination of equalization is a challenge which further complicates the validation process and increases the likelihood of not achieving the best performance in device testing.

Conformance Testing

Conformance testing of high-speed data links starts with separately verifying the transmitter (Tx) output and the receiver (Rx) input performance. Test boards or special fixtures may be used to access the test signals and for some tests an actual channel (or a model of a channel) may be included in the setup. In multi-lane interfaces such as 200GAUI-2, 400GAUI-4 one lane is tested at a time, generally with signals present on the other lanes to account for the effects of crosstalk within the device and channel being tested.

Standards define the conformance test points for each link. Figures 3, 4 and 5 show how the test points are defined in IEEE 802.3. Chip-to-module testing employs the use of defined test fixtures – a host compliance board (HCB) and a module compliance board (MCB). Chip-to-chip and backplanes use a custom printed circuit board to bring out the test signals to a suitable connector. Copper cable testing uses a specified test cable assembly with mated connectors. Transmitter and receiver specifications for each interface take into account the effect of these test fixtures and boards.

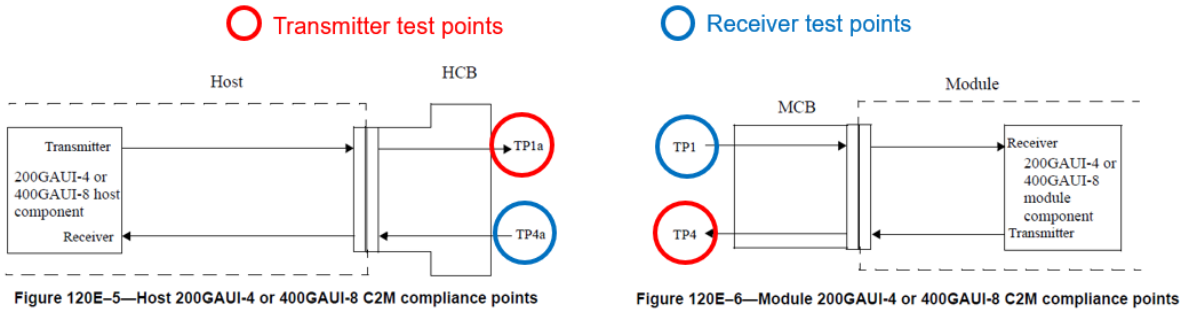

Figure 120E–5—Host 200GAUI-4 or 400GAUI-8 C2M compliance points

Figure 120E–6—Module 200GAUI-4 or 400GAUI-8 C2M compliance points

Figure 3. Compliance test points for C2M host, C2M module measurements [3]

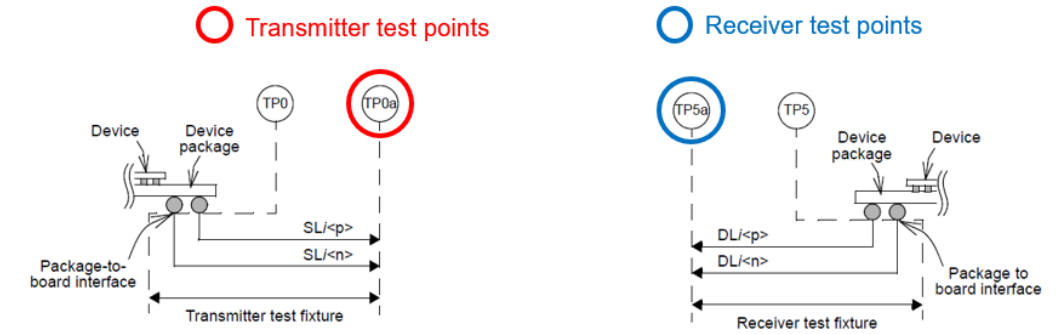

Figure 93–5—Transmitter test fixture and test points

Figure 93–10—Receiver test fixture and test points

Figure 4. Compliance test points for C2C / KR measurements [3]

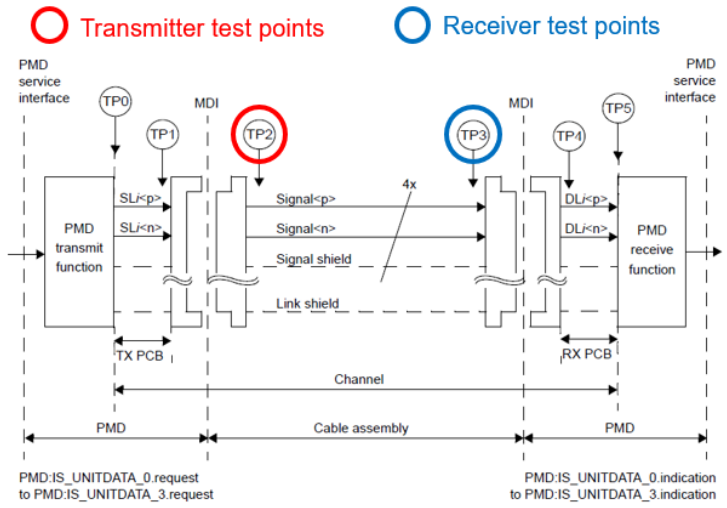

Figure 92–2—100GBASE-CR4 link (one direction is illustrated)

Figure 5. Compliance test points for CR measurements [3]

[3] IEEE Std 802.3-2018, IEEE Standard for Ethernet

For conformance testing, both the Tx and Rx tests employ the concept of a reference receiver. The transmitter performance is qualified when driving into an ideal reference receiver. This reference receiver is modelled in a high-speed oscilloscope with defined bandwidth and equalization parameters. In order the create the ideal reference receiver it is essential for the oscilloscope to be able to lock to the pattern and be able to handle the pattern length for data processing, so usually short patterns such as PRBS13Q or PRBS9Q are used for the oscilloscope measurements.

Transmitter parameters are measured at the output of the reference receiver's equalization circuits. Receiver performance test uses an impaired signal to simulate worst-case conditions at the receiver input. This impaired signal is first calibrated using an oscilloscope with the same reference receiver model and many of the same parameter measurements.

Each of the interfaces and reaches have different test requirements and key parameters, requiring a diverse test suite to characterize all link options.

Transmitter test

Most transmitter tests are performed by connecting the transmitter output directly to a high-speed oscilloscope with cables or test fixtures. For Tx return loss measurements, a network analyzer or time-domain reflectometer (TDR) solution may be required.

Generally, the transmitter's own equalization / de-emphasis should be optimized first, usually for maximum eye opening or minimal VEC. Then the reference receiver's equalization is optimized. Achieving the optimum receiver equalization settings is not a simple task, as there can be multiple minima. And since margins are reduced in 100G / lane links it is essential for compliance testing to be able to achieve the correct equalization settings for the best performance.

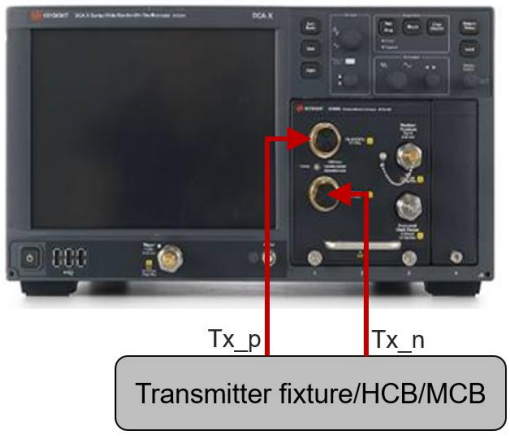

Figure 6. Transmitter measurements with oscilloscope

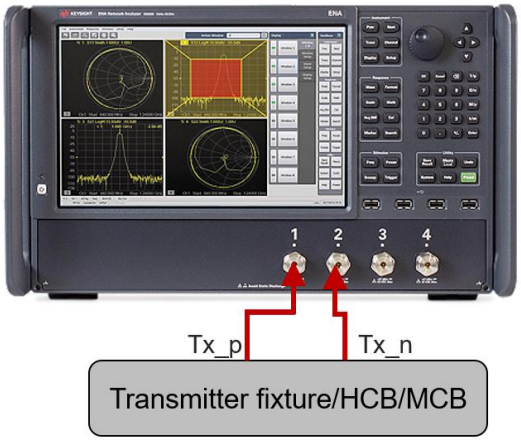

Figure 7. Transmitter measurements with network analyzer

For measurements such as eye height, eye width and vertical eye closure the measurement procedure is quite complex, requires advanced analysis methods and is only practical with automation in the test process. Figure 8 shows the test measurement flow for C2M transmitter testing as defined in IEEE 802.3ck.

Today's high-speed oscilloscopes include many of the measurements required e.g. eye height, VEC, SNDR etc. It is vital that these measurement algorithms are also kept up to date to ensure accurate measurements when qualifying a device.

C2C

Typical Tx tests for C2C, KR, CR, MR and LR include output voltage in both the enabled and disabled states, common mode voltages, return loss, differential steady state voltage, linear fit pulse response, PAM4 levels linearity, de-emphasis cursors, SNDR and Jitter (Jrms, J3u/J4u/J5u, EOJ).

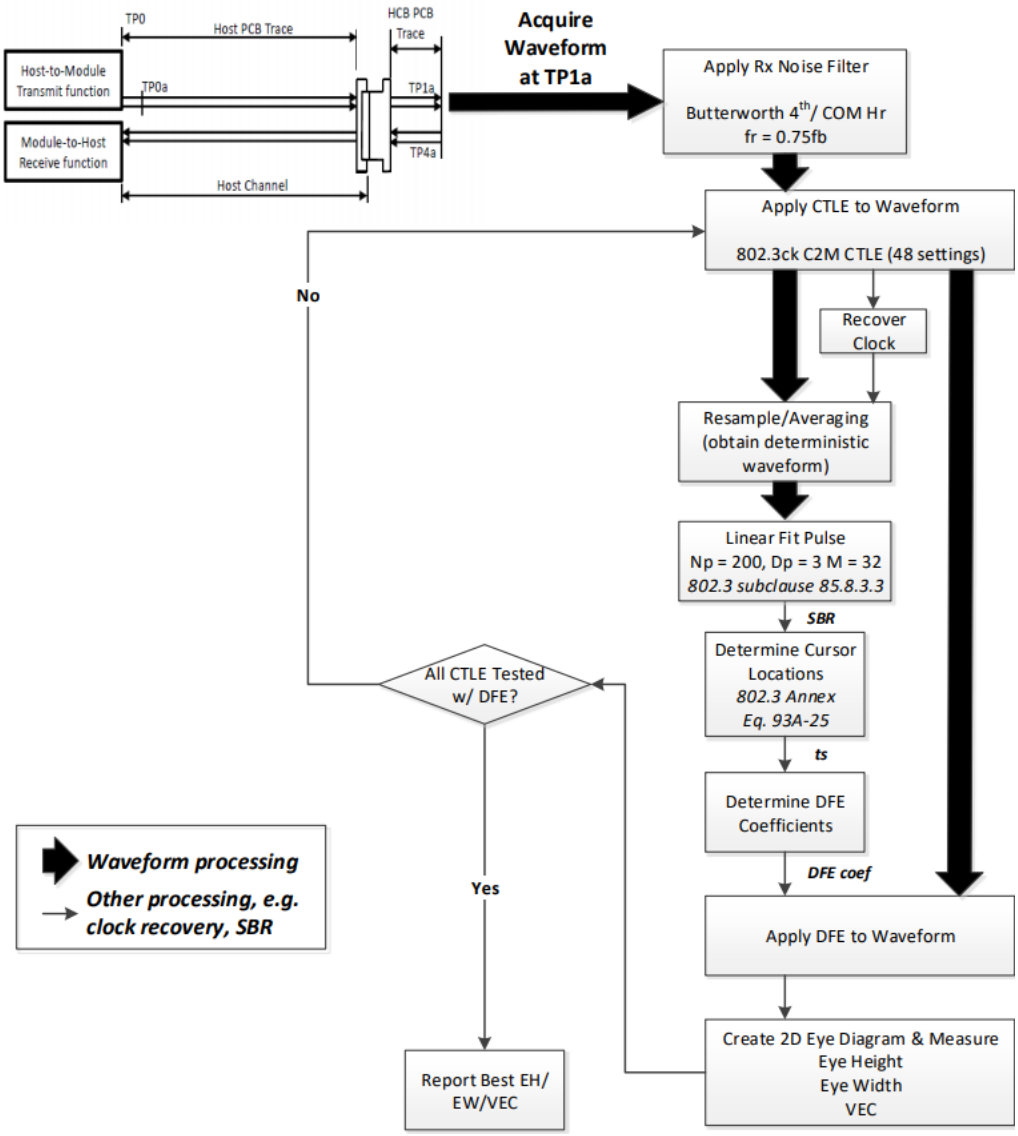

Figure 8. C2M Tx test measurement flow [4]

[4] 802.3ck C2M TP1a Compliance Test Measurement Flow - https://www.ieee802.org/3/ck/public/19_11/li_3ck_02_1119.pdf

C2M

C2M and VSR testing includes output voltage enabled/disabled, common mode voltages, return loss, termination mismatch, eye height, VEC and transition time. Test requirements are different at both ends of the link – host or module.

Eye measurements at TP1a are the most important for C2M host transmitter testing. This requires several key components in the reference receiver such as a 4th order Butterworth filter, CTLE and DFE equalization and a defined noise spectral density 4.10E-8 V2/GHz as shown in Figures 9 and 10. Before starting the eye measurements, the optimal equalizer settings need to be achieved. An equalization tuning process is required to measure EH and VEC at up to 64 combinations of CTLE plus DFE settings. Once the optimal equalizer settings are determined, these settings will be used for the transmitter eye measurements.

Figure 9. Reference receiver noise and equalizer components

A similar process is used for the module transmitter testing, except that the output should be qualified for both short and long module output modes. In addition, testing should use both near-end and far-end host channels for a total of four test configurations. To achieve this, the signal measured at TP4 for each mode is first convolved with the near-end or far-end host channel s-parameter file before the eye measurements are taken. Equalization is optimized for each different test configuration.

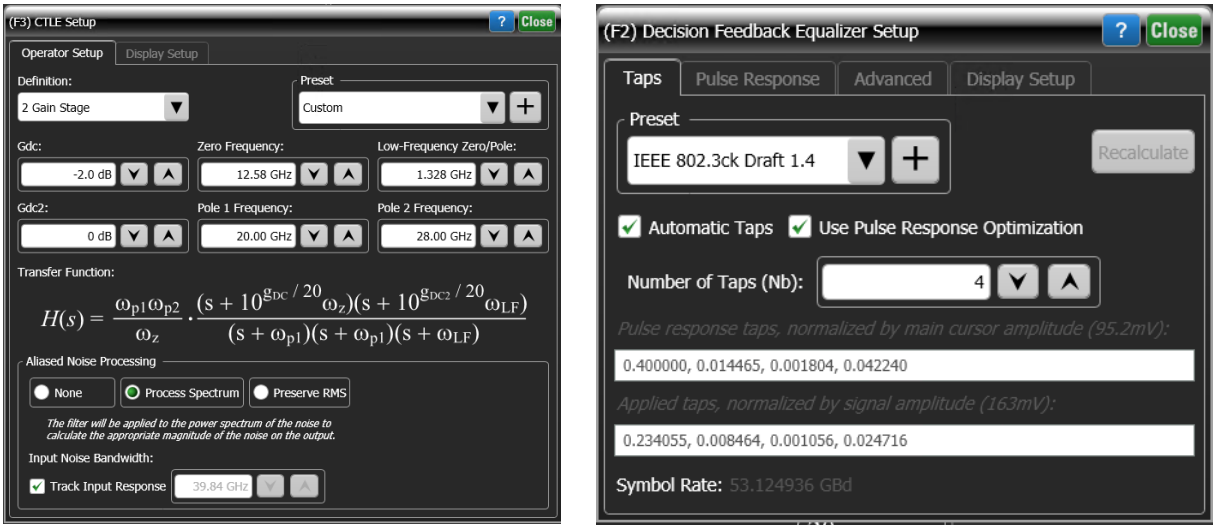

Figure 10. CTLE and DFE settings

Receiver test

Conformance testing of receivers requires additional equipment: a high-speed PAM4 pattern generator, noise source, channel printed circuit board, oscilloscope, and error analyzer. Unlike transmitter test where the signal from the transmitter is directly measured, receiver testing involves applying a stressed or impaired signal to the receiver input. This signal represents the worst-case signal arriving at the receiver from a compliant transmitter plus compliant channel. In the presence of the stressed signal the receiver must be able to equalize and re-sample the signal with a resulting bit error ratio below the specified limit from the standard. Table 2 shows the BER requirements for the various 800G interfaces.

Table 2. Pre-FEC and post-FEC BER requirements

Interface	BER targets	Frame loss ratio
CR1, KR1	2.4×10^{-4}	6.2×10^{-10}
CR2, CR4, KR2, KR4	2.4×10^{-4}	6.2×10^{-11}
C2C [5]	1.0×10^{-5}	
C2M	1.0×10^{-5}	
VSR, MR	1.0×10^{-6}	1.0×10^{-15}
LR	1.0×10^{-4}	1.0×10^{-15}

Receiver conformance testing is generally done without any forward error correction (FEC) being applied, but with the caveat that the error distribution should be random enough such that when FEC is applied, the resulting post-FEC BER or frame loss ratio (FLR) will be below its specified level. However, the use of adaptive equalization and DFE in receivers can introduce burst errors into the transmission, and it is recommended to perform receiver testing with both PRBS signaling as well as under FEC conditions to establish the actual FLR and FEC margin.

The first step in receiver conformance testing is to calibrate the stressed signal. There are different methods depending on the interface being tested.

C2C

Chip-to-chip receiver testing is based on the Channel Operating Margin (COM) [6] method. The COM figure of merit is calculated mathematically from models of the transmitter and receiver circuit board traces and s-parameter measurements of the channel. COM is basically a measure of signal-to-noise ratio at the receiver input.

[5] Higher BER allowed if scrambled idle pattern used instead of PRBS13Q
[6] Channel Operating Margin – IEEE 802.3-2018, IEEE Standard for Ethernet, Annex 93A

First the pattern generator is characterized using an oscilloscope, measuring many of the same parameters and setting equalization methods as the transmitter tests. Next an analysis of the setup is performed to establish the COM value and then additional noise is added to achieve the required COM value for receiver testing (usually COM = 3.0 dB for receiver test). This analysis requires s-parameter models of the channel and Tx / Rx package traces – this can be a combination of measured and synthesized values, concatenated together.

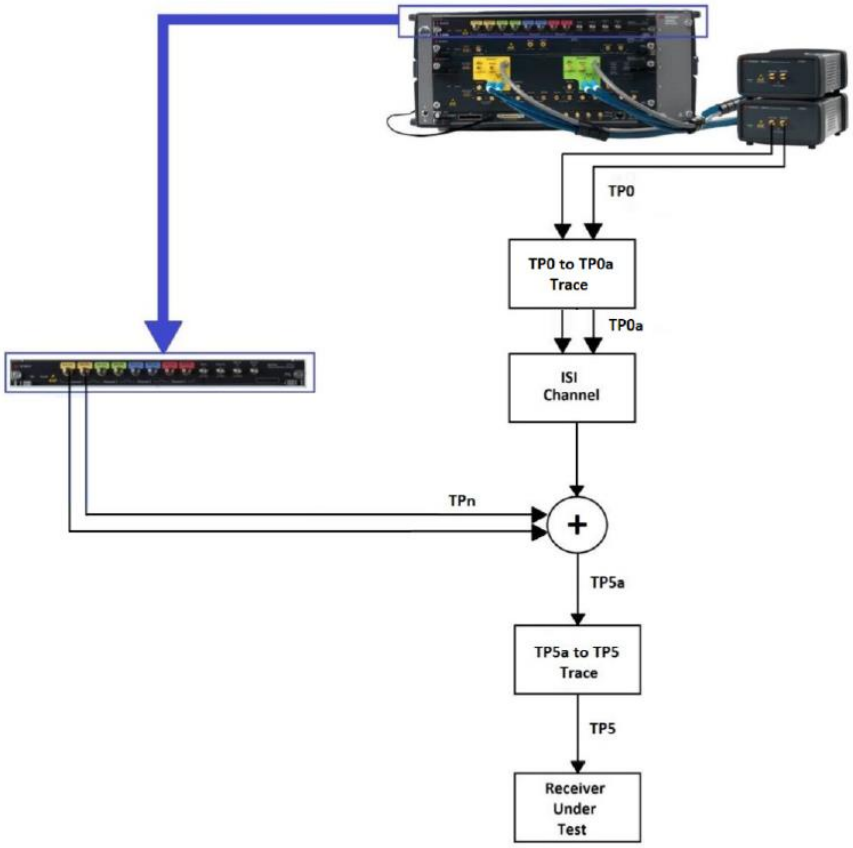

Figure 11. Setup for C2C test

Once the system is fully calibrated, connections to the receiver-under-test are made and an Interference Tolerance test and Jitter Tolerance test are performed on the receiver. Interference tolerance determines if the receiver can meet the BER specification in the presence of the stressed signal with COM = 3.0 dB. Jitter tolerance test involves sweeping the pattern generator's sinusoidal jitter over a specified range of frequencies and amplitudes to test the receiver's clock recovery circuit and is performed with no added noise. Two sets of calibrations and tests are required for the low loss (10 dB) and high loss (20 dB) channels.

C2M

Chip-to-Module conformance test uses the Stressed Eye method. Like C2C, the C2M setup requires a pattern generator, crosstalk source, frequency dependent attenuator (printed circuit board traces), an oscilloscope and error analyzer. The calibration requires adding jitter, ISI, and crosstalk to meet stressed parameters of EH and VEC. Separate calibrations and tests are required depending on whether the Host input or Module input is being tested.

First, the crosstalk generator is calibrated using a mated pair of HCB/MCB (Host Compliance Board / Module Compliance Board). Figure 12 shows the setup for C2M Host input; the crosstalk signal is applied at TP4a but calibrated at TP4.

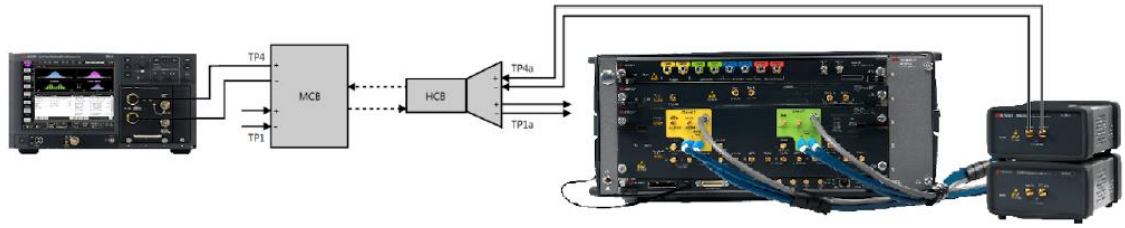

Figure 12. Setup for C2M Host calibration of crosstalk signal

The stressed eye calibration is performed with the previously calibrated crosstalk signal applied. Figure 13 shows the test setup for C2M Module input. The stressed eye is applied at TP1 but calibrated at TP1a. It is important to use compliant HCB and MCB for these calibrations.

Once calibrated the HCB/MCB are separated and the receiver-under-test is connected to either the HCB (for Host input test) or the MCB (for Module input test). The standard conformance test is a Jitter Tolerance test, sweeping the pattern generator's sinusoidal jitter with the other stresses applied. The receiver-under-test must meet the BER target during this test.

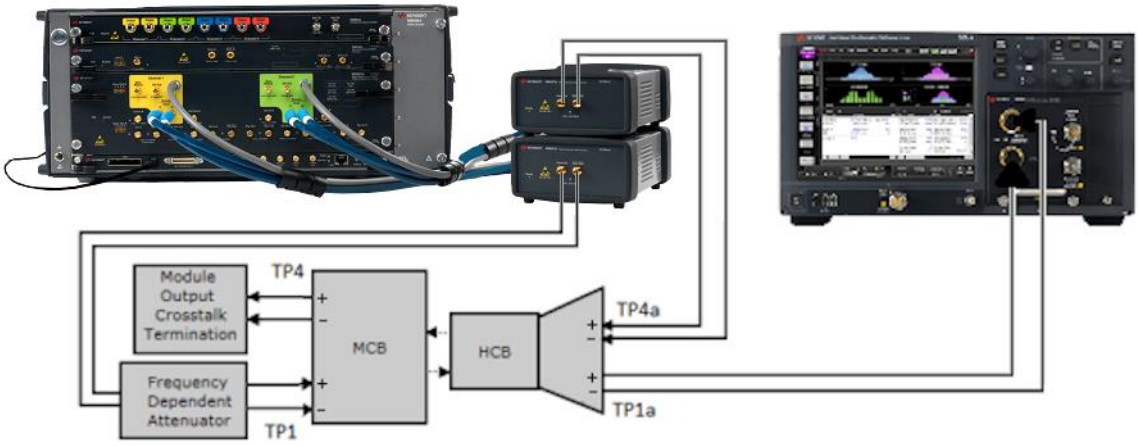

Figure 13. Setup for C2M Module input Stressed Eye calibration

C2M Module input conformance testing is done for short (low loss) and long (high loss) channels. The short channel test requires just the HCB/MCB combination while for the long channel, frequency dependent attenuation is added such that the total channel loss is 16-18 dB. This requires additional stressed signal calibration and JTOL test for each channel.

Keysight Test Solutions

Setting up conformance tests for 53 Gbaud PAM4 links is complicated and time-consuming, and requires time, experience, and attention to details to get efficient, repeatable, accurate calibrations and measurements of Tx and Rx parameters. In addition to providing the oscilloscope and bit error ratio measurement instruments capable of running such tests, Keysight Technologies also offers several software test solutions for IEEE 802.3ck and OIF-CEI-112G interfaces with the following benefits:

- Guided setups and measurements
- Connection diagrams
- Control of all necessary equipment
- Automated stress signal calibration for Rx testing
- Auto tuning process for CTLE, DFE
- HTML reports and export of results
- Data analytics ready
- Test sequencer
- Remote control interface

For each test selected the conformance pass/fail limits are pre-loaded but can also be easily modified by the user to explore design margins or debugging issues. Other parameters such as signaling rate, equalization settings, parameters related to measurement computation etc. are fully customizable in the solutions configuration.

Transmitter test solutions

Transmitter test solutions are available for both the N1000A DCA-X Wide-bandwidth Oscilloscope and the Infiniium UXR-series Real-time Oscilloscope.

Solution	Standard covered	Reach/Link	Available on
N1091CKCA	IEEE 802.3ck	C2C, C2M, KR, CR	DCA-X
N109212CA	OIF-CEI-112G	VSR, MR, LR	DCA-X
D90103CKC	IEEE 802.3ck	C2C, C2M, KR, CR	UXR-series
D9050CEIC	OIF-CEI-112G	VSR, MR, LR	UXR-series

For the selected standard the full list of tests is available. These can be run individually or selected as a group. The application will perform the tests in sequence, prompting the user whenever a configuration change is required. Figure 14 shows an example test list for C2C/C2M testing.

Figure 15 shows a screen shot from the UXR oscilloscope. The upper waveform is the raw PAM4 signal from the transmitter. In the lower waveform the PAM4 eye has been opened up using CTLE and DFE equalization in the reference receiver.

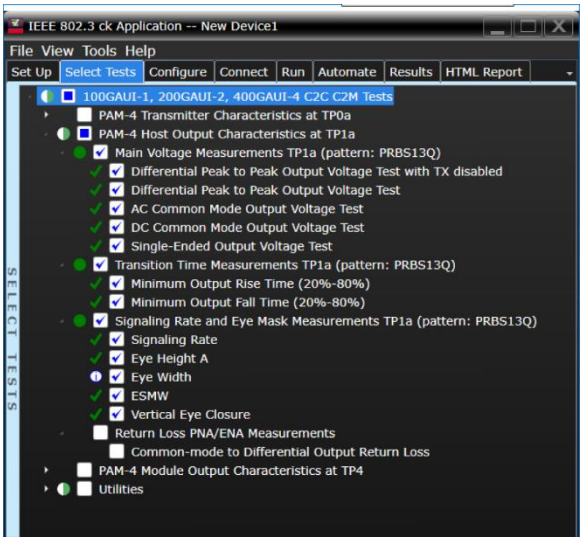

Figure 14. Test selection for Tx measurement

Figure 15. Running a Tx test on the UXR

Test results are presented both in tabular form or in html report format, showing measured value, specification limit and margin.

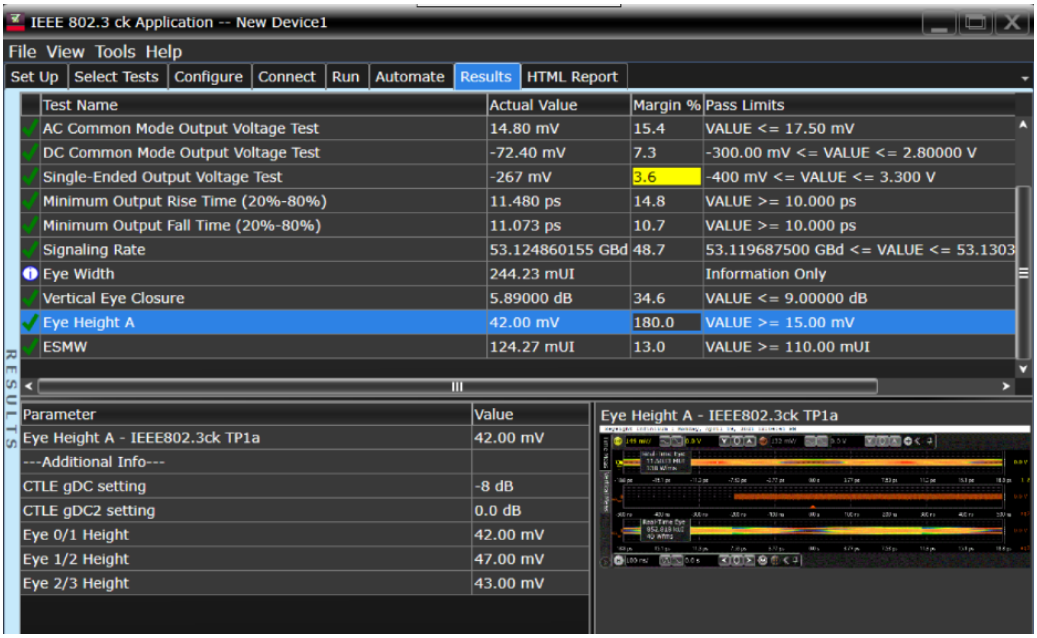

Figure 16. Test results for Tx measurements

Receiver test solutions

Receiver test solutions are available supporting the M8040A 64 Gbaud or M8050A 120 GBaud High-performance BERT plus the N1000A DCA-X wide-bandwidth oscilloscope and the Infiniium UXR-series real-time oscilloscopes.

The first receiver conformance test solution released for 100G / lane is the M8091CKCA. covering IEEE 802.3ck. A solution supporting OIF-CEI-112G is the M809212CA.

Solution	Standard covered	Reach/link
M8091CKCA	IEEE 802.3ck	C2C, C2M
M809212CA	OIF-CEI-112G	VSR, MR, LR

Connection diagrams guide the user through each calibration and device test step. Results of calibration and device test are displayed, again with measured and specification limits.

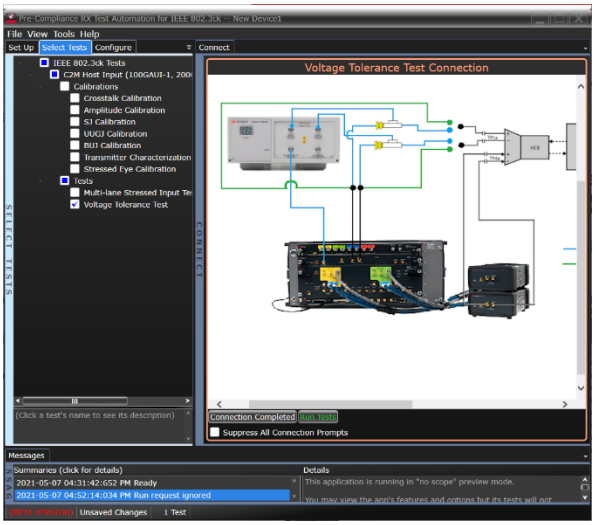

Figure 17. Connection setup for Rx test

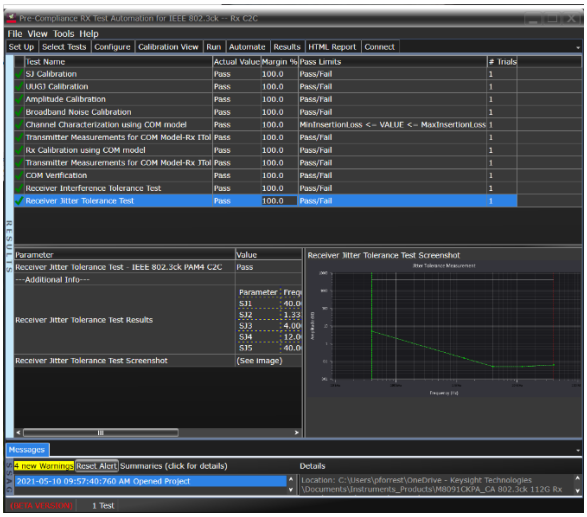

Figure 18. Test results for Rx measurement

For more information on 800G conformance test applications and other 800G test solutions visit Keysight Technologies 800G Solutions web page at www.keysight.com/find/800G

Conclusion

As link speeds and data rates increase to meet demand, channel losses and test margins reduce. The requirements to successfully characterize these links necessitate more complex measurement setups, detailed analysis, and processing of measured data, resulting in a potentially time-consuming and error-prone process if attempted manually. Effective validation of devices and interfaces can only be efficiently achieved with a robust and accurate test regime.

Keysight's unique position in collaborating with the IEEE 802.3 and OIF-CEI standards organizations allows for the release of the industry's first Tx and Rx automated conformance test solutions well before the latest 800G standards are fully released, with periodic updates as the standards progress through their evolution.